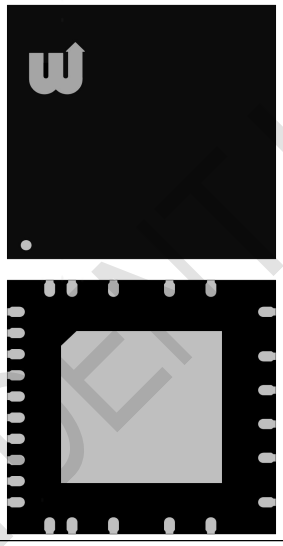
Application

- Fail operational power supply targeting high current applications
- Connection/isolation switch between power supplies (e.g. for hybrids and electric vehicles)
- Developed to support dependable power supply and distribution

Package	QFN6×6-26
Marking	WS2510AT



Basic Features

- AEC-Q100 qualified
- ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- One channel device with two high-side gate driver outputs
- 3 Ω pull-down, 50 Ω pull-up for fast switch on/off
- Support back-to-back MOSFET topologies (common drain and common source)
- Two bidirectional high-side analog current sense interfaces with externally adjustable gain
- Adjustable overcurrent/short-circuit protection
- Versatile comparator to implement: adjustable I-t wire protection, overvoltage/undervoltage or overtemperature protection

AEC Qualified

ISO 26262 ready

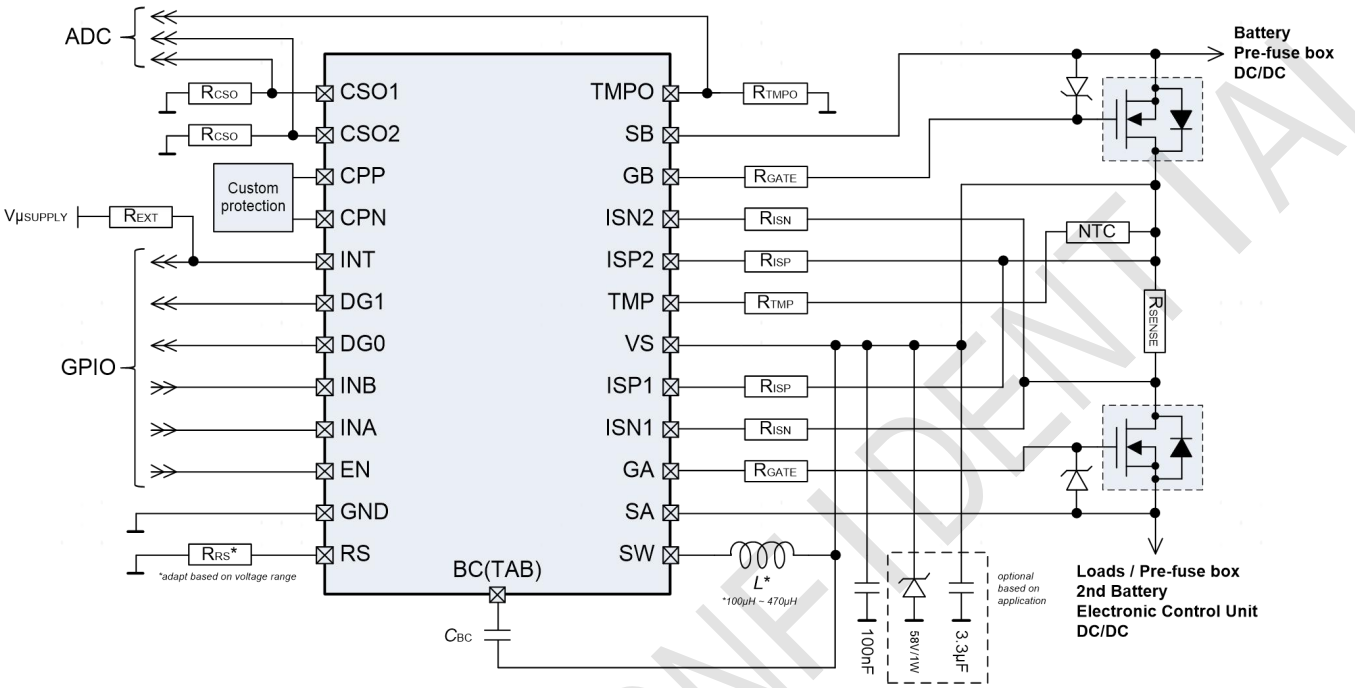
RoHS

Halogen-free

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_S	100V
Operating voltage range	$V_{S(NOR)}$	8-72V
Operating voltage extended range	$V_{S(EXT)}$	3-100V
CSA adjustable gain	G	10~200
Gate turn on short circuit pulsed current per gate	$I_{G(ON)}$	175mA
Gate turn-off short circuit pulsed current per gate	$I_{G(OFF)}$	1400mA
Turn on delay	$I_{D(ON)}$	4us @ C_G=100nF
Turn off delay	$I_{D(OFF)}$	4us @ C_G=100nF
GND current in SLEEP mode	$I_{GND+RS(SLEEP)}$	1~15uA
BC current in IDLE mode	$I_{BC(IDLE)}$	5~50uA

Typical Application Circuit

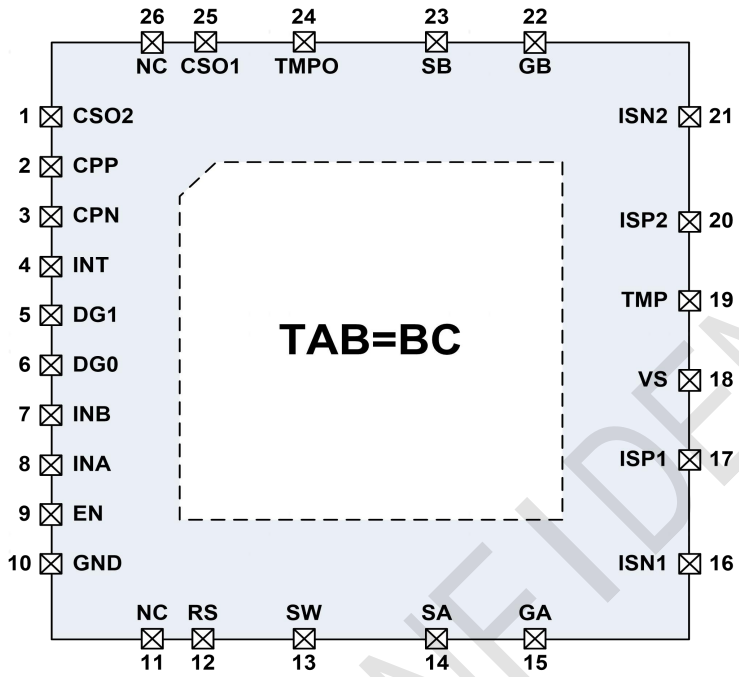


Ordering Information

Package	Top Mark	Part No.
QFN6×6-26, Pb-free	WS2510AT XXYMXX	WS2510AT

Pin Configuration

Top view



Pin Description

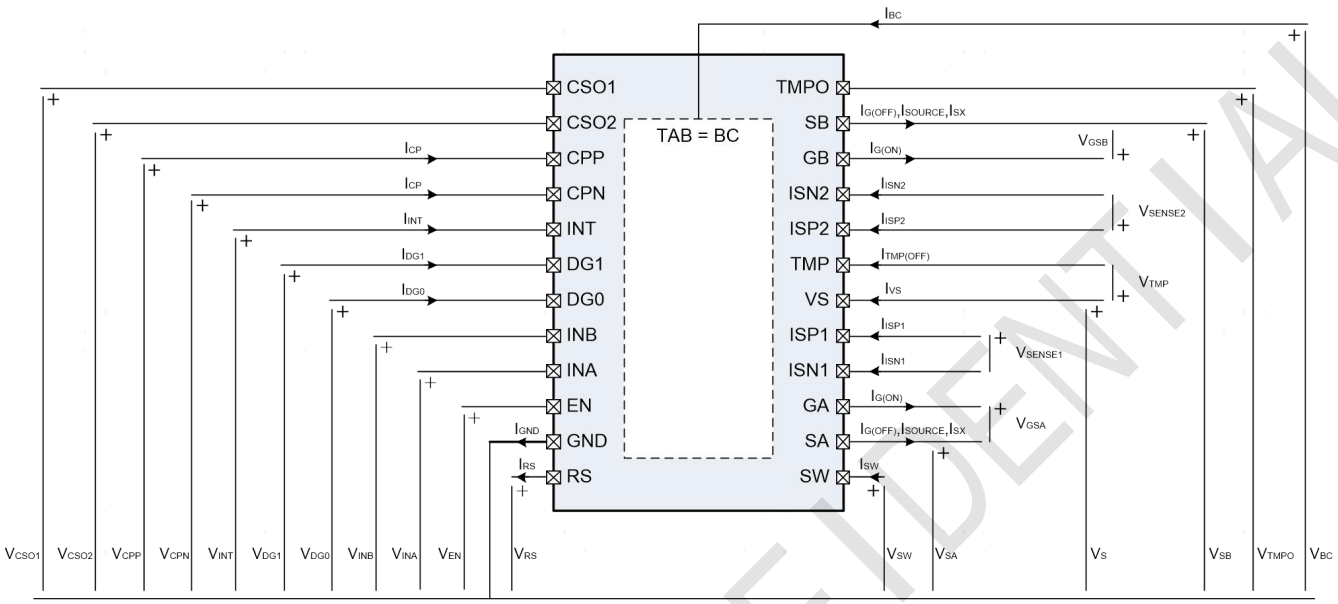
Pin Name	Pin NO.	Pin Description
CSO2	1	Current Sense Output 2: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP2/ISN2.
CPP	2	Comparator Positive: analog positive input of comparator.
CPN	3	Comparator Negative: analog negative input of comparator.
INT	4	Interrupt: open drain interrupt output.
DG1	5	Diagnostic 1: DG1 is logic low in SLEEP mode and IDLE mode. Digital voltage information of current flow direction in ON mode: • DG1 is logic high if current flows from ISP1 to ISN1 connection • DG1 is logic low if current flows from ISN1 to ISP1 connection Digital voltage information in SAFESTATE mode: • DG1 is logic high if SAFESTATE because of CP or SC or VS(UV) • DG1 is logic low if SAFESTATE because of UVLO
DG0	6	Diagnostic 0: DG0 is logic low in SLEEP mode and IDLE mode. Digital voltage information of boost converter frequency in ON mode. Digital information in SAFESTATE mode: • DG0 is logic high if SAFESTATE because of CP or UVLO • DG0 is logic low if SAFESTATE because of SC or VS(UV)

INB	7	Input B: If INB digital logic is low, channel B switches OFF. If INB digital logic is high, channel B switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
INA	8	Input A: If INA digital logic is low, channel A switches OFF. If INA digital logic is high, channel A switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
EN	9	ENABLE: If EN digital logic is low, gate driver is in SLEEP mode, channels A and B are switched OFF and gate driver is RESET. If EN digital logic is high, gate driver is in IDLE mode when INA and INB are both logic low.
GND	10	Ground connection.
NC	11	NC
RS	12	Resistor sense output of boost converter: current measurement of the boost converter.
SW	13	Switching supply input of boost converter. Inductance connection.
SA	14	Source A: output A connection to external MOSFET sources.
GA	15	Gate A: output A connection to external MOSFET gates.
ISN1	16	I Sense Negative 1: external shunt or VDS negative connection.
ISP1	17	I Sense Positive 1: external shunt or VDS positive connection.
VS	18	Voltage reference, extended 3 V to 100 V.
TMP	19	Temperature Input: analog connection to external NTC or PTC thermistor.
ISP2	20	I Sense Positive 2: external shunt or VDS negative connection.
ISN2	21	I Sense Negative 2: external shunt or VDS positive connection.
GB	22	Gate B: output B connection to external MOSFET gates.
SB	23	Source B: output B connection to external MOSFET sources.
TMPO	24	Temperature Output: analog voltage feedback provides a voltage proportional to thermistor temperature.
CSO1	25	Analog voltage to force SAFESTATE mode. Current Sense Output 1: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP1/ISN1.
NC	26	NC
BC	TAB	Boost Converter output capacitor connection; driver supply.

Table 1. Suggested connections for unused and not connected pins

Pin Name	Pin NO.	How to connect pin to disable corresponding function
CSO2	1	GND
CPP	2	GND (FLOAT can trigger random latch CPP)
CPN	3	EN (VS induces 'large' current consumption. GND can trigger random latch)
INT	4	FLOAT
DG1	5	FLOAT
DG0	6	FLOAT
INB	7	GND (FLOAT potential IBC increase, DPI sensitivity increased if SB GB floating, no IDLE mode)
INA	8	GND (FLOAT potential IBC increase, DPI sensitivity increased if SA GA floating, no IDLE mode)
EN	9	5V (@GND driver will always remain in SLEEP mode. EN can also be connected to VS with 100k+diode so driver is by default in IDLE mode as long as a power supply is connected > Vzener+Vrev_diode is present on VS pin. diode: cathode on VS.)
GND	10	GND (never leave open: can randomly activate boost converter, IC destruction))
NC	11	FLOAT
RS	12	FLOAT (when using external supply directly on BC, RS connection to GND could cause IC destruction)
SW	13	FLOAT (in case of boost supply converter disconnection and driver external supply directly on BC)
SA	14	FLOAT (if GA not used)
GA	15	FLOAT
ISN1	16	GND
ISP1	17	VS
VS	18	VS (FLOAT: BC is not regulated, external MOSFET gate destruction expected).
TMP	19	FLOAT
ISP2	20	VS
ISN2	21	GND
GB	22	FLOAT
SB	23	FLOAT (if GB not used)
TMPO	24	FLOAT or GND
CSO1	25	GND (FLOAT can trigger random latch on CSO1 internal comparator)
NC	26	FLOAT
BC	TAB	Boost capacitor C_{BC} or external supply (see datasheet for V_{BC}-V_S functional range.

Current and Voltage Conventions



Note1：

1) Voltages are defined positive with respect to ground.

2) Currents are defined flowing into or from the pin depending on pins.

Absolute Maximum Ratings (Note2)

Symbol	Parameter	Value	Unit
V_{BC}	Maximum voltage VBC (boost converter output)	-0.3 to 120	V
V_{BC_VS}	Boost voltage with respect to VS	-0.3 to 15	V
V_S	Maximum voltage VS	-0.3 to 100	V
V_S - V_{SX}	Maximum drain-source voltages on each output	-36- to 120	V
V_{GX} - V_{SX}	Maximum voltage between gate and source pins on each output	-0.3 to 120	V
V_{BC}-V_{GX}	Maximum voltage BC to GX	-0.3 to 120	V
V_{BC}-V_{SX}	Maximum voltage BC to SX	-0.3 to 120	V
V_{BC}-V_{ISPX}	Maximum voltage BC to ISPx	-0.3 to 120	V
V_{BC}-V_{ISNX}	Maximum voltage BC to ISNx	-0.3 to 120	V
V_{CSOX}	CSOx voltage	-0.3 to 5.5	V
V_{EN} V_{INA} V_{INB} V_{CPP} V_{CPN}	Logic input voltages(EN,INA,INB,CPP,CPN)	-0.3 to 5.5	V
V_{DGX}	DGx voltage	-0.3 to 5.5	V
V_{TMP}	Temperature input: analog connection to external NTC or PTC thermistor.	-0.3 to 100	V
V_{TMPO}	Temperature output: analog voltage feedback provides a voltage proportional to thermistor temperature.	-0.3 to 5.5	V
V_{SW_RS}	Maximum voltage between SW and RS pin	-0.3 to 120	V
I_{SW}	Maximum pulsed current in SW pin	200	mA
$T_{J(MAX)}$	Maximum operating junction temperature	-40 to 150	℃
$T_{STG(MAX)}$	Storage temperature	-55 to 150	℃

Note2：

1) Not subject to production test - specified by design.

2) Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Functional Ranges (Note3)

-40°C < T_j < 150°C, all voltages with respect to ground, typical values are given for V_S = 14 V and T_J = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{S(NOR)}$	Voltage reference range for normal operation	8	-	72	V
$V_{S(EXT)}$[2)]	Voltage reference extended range	3	-	100	V
$V_{S(SC)LOW}$	Voltage reference range with lower short-circuit protection	3	-	8	V
V_{EN}, V_{INA}, V_{INB}	Input pins EN, INA, INB	0	-	5.5	V
V_{DG0}, V_{DG1}[3)]	Diagnostic pins DG0, DG1	0	-	k_{DG}*V_{EN}	V
V_{INT}	Interrupt pin INT	0	-	5.5	V
$V_{CP(REF)}$	Comparator reference voltage pins CPN, CPP	1	-	5.5	V
$V_{AMP(SAT)}$[4)]	Analog output pins saturation CSO 1&2, TMPO	3.9	4.6	5.5	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
$G^{5)}$	Current sense amplifiers gain range	10	-	200	-
V_{BC}-V_S	Supply voltage range for amplifier operation	6	-	15	V
V_{BC}-V_{ISxx}	Amplifier input voltage range	6	-	15	V
$V_{ISxx\text{-}GND(TH)}$	Amplifier input voltage threshold for disconnection	0.2	0.7	1.5	V

Note3：

1) Not subject to production test - specified by design.

2) Parameter deviations possible

3)See k_{DG} parameter

4)$V_S = V_{S(NOR)}$

5)For G ≤ 30, use only R_{CSO} = 10 kΩ

Thermal Resistance (Note3)

Symbol	Parameter	Value	Unit
T_{JA}	Thermal Resistance Junction-to-Ambient	27	K/W

Note3：

1) Not subject to production test - specified by design.

ESD Susceptibility (Note4)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}^{2)}$	ESD HBM susceptibility all pins	±2	kV
$V_{ESD(CDM)}^{3)}$	ESD CDM susceptibility all pins	±500	V
$V_{ESD(CDM)}^{4)}$	ESD CDM susceptibility corner pins (pins 1, 12, 13, 24)	±750	V

Note5：

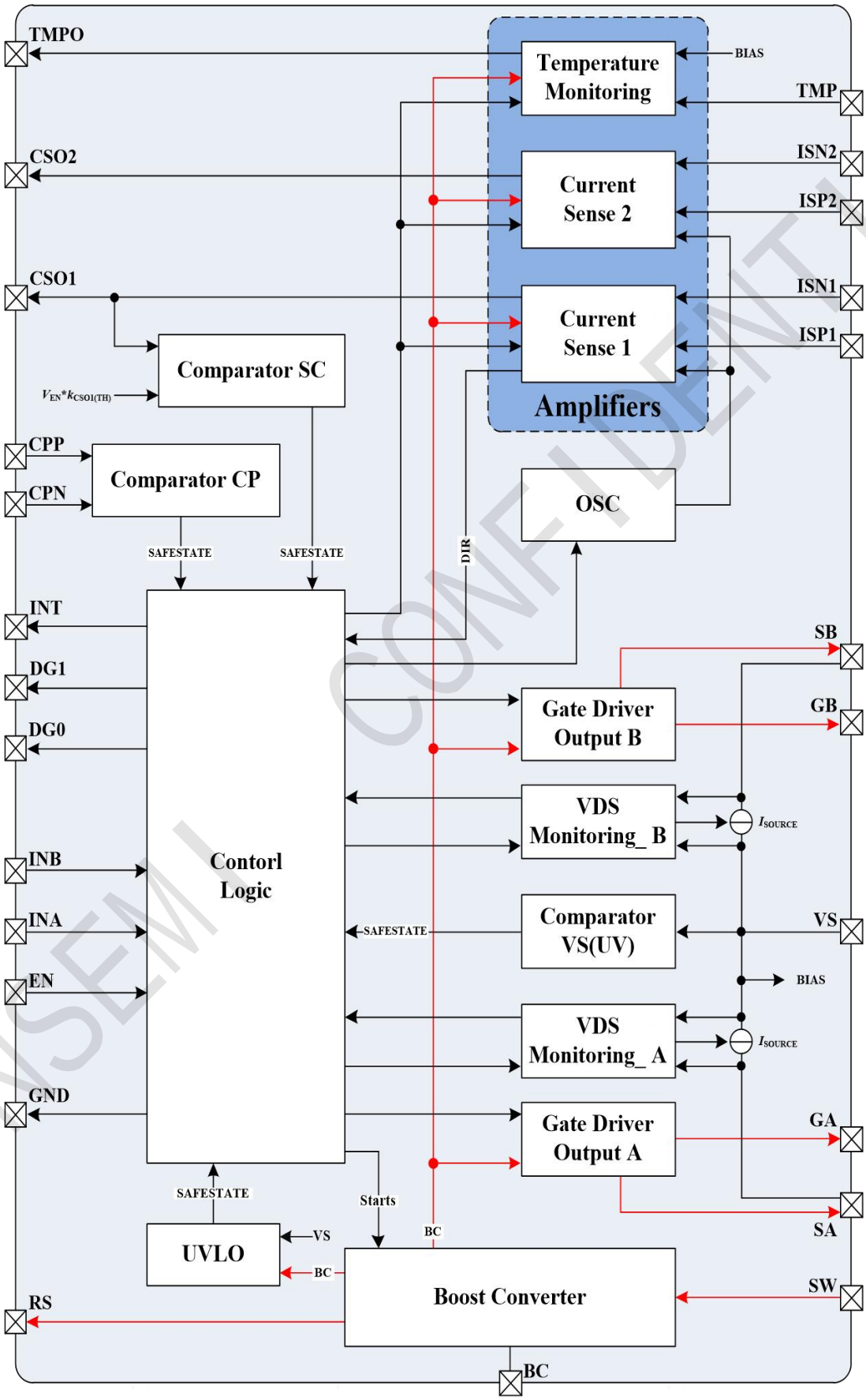
1) Not subject to production test - specified by design.

2) ESD susceptibility, Human Body Model “HBM”, according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

3) ESD susceptibility, Charged Device Model “CDM”, according to ANSI/ESDA/JEDEC JS-002.

4) ESD susceptibility, Charged Device Model “CDM”, according to ANSI/ESDA/JEDEC JS-002.

Functional Block



Electrical Characteristics (Note6) , 8V< V_S < 72 V; -40°C < T_j < 150°C, unless otherwise specified

Inputs pins

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input A,B & Enable voltage high level	$V_{IN(H)}$, $V_{EN(H)}$	–	2.5	–	–	V
Input A,B & Enable voltage low level	$V_{IN(L)}$, $V_{EN(L)}$	–	–	–	0.7	V
Input A,B & Enable pull-down internal resistor	$R_{IN(GND)}$	–	0.5	1.5	2.5	MΩ
Input zener diode for local pins	$V_{Z(IN)}$ 2)	–	5	5.5	6	V

Digital diagnostic pins

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Ratio diagnostic pin voltage high level over V_{EN}	$k_{DG(H)}$	–	0.9	1	1.1	–
Diagnostic pin voltage low level	$V_{DG(L)}$	V_{BC} = 120 V	–	–	0.1	V
Diagnostic pin serial resistor	$R_{DG(GND)}$	–	5	10	20	kΩ
Delay for current direction change on DG1	t_{ISD}	Indicates current flow direction change on CSA1 only ON mode only	0	15	50	µs
Interrupt pin pull-down internal resistor, SAFESTATE active	R_{INT}	–	5	10	20	kΩ
Interrupt pin current leakage	$I_{INT(NOSAFESTATE)}$	$V_{INT(H)}$ ≤ 5.5 V	–	–	0.3	µA

Comparator (CP)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Comparator offset	$V_{CP(OFFSET)}$	$V_{CP(REF)MIN}$ ≤ $V_{CP(REF)}$ ≤$V_{CP(REF)MAX}$	-50	–	50	mV
Comparator leakage input current	I_{CP}	V_{CP} = 5.5 V	-100	–	500	nA

Temperature amplifier (TMPA)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
TMPA input current	$I_{TMP(OFF)}$	–	-100	–	100	nA
TMPA input offset	$V_{TMP(OFFSET)}$	–	-10	0	10	mV
TMPA ratio	k_{TMP}	–	9.5	10	10.5	–
TMPA pull-down resistor	R_{TMPO} 2)	–	20	–	100	kΩ

Current sense amplifiers (CSA1 & CSA2)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CSA input offset	$V_{ISx(OFFSET)}$ 2)	–	-50	0	50	µV
CSA input blind range	$V_{ISx(BLIND)}$	–	-500	0	500	µV
CSA delay maximum accuracy	$t_{CSA(ACC)}$	–	0	200	400	µs
CSA settling time	$t_{CSA(SET)}$ 2)	Step 25% , G=100	1	92	236	µs
CSA output pull-down resistor	R_{CSOx} 2)	–	10	20	50	kΩ
CSA gain intrinsic error	$\varepsilon_{(G)}$ 2)	G = 10..200,Vsense>3mV	-1	0	1	%
CSA gain intrinsic error	$\varepsilon_{(G)}$ 2)	G = 10..200,Vsense≤3mV	-5	0	5	%

PSRR - CSA power supply rejection ratio	$PSRR_{1kHz}$[3]	f = 1 kHz, G = 100,R_{CSO} = 20 kΩ、	–	105	–	dB
CMRR - CSA common mode rejection ratio	$CMRR_{1kHz}$[3]	f = 1 kHz, G = 100, R_{CSO} = 20 kΩ、	–	116	–	dB
Noise - CSA Voltage noise, RTI	$Noise$[3]	G = 100, R_{CSO} = 20 kΩ RTI	–	180	–	nV_{RMS}

Protection thresholds

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current shutdown internal threshold ratio from Enable pin voltage	$k_{CSO1(TH)}$	V_S = 8 V to 72 V ON mode, CSA1 only	0.71	0.74	0.77	–
Under voltage threshold	$V_{S(UV)}$	V_S - GND ON mode only	0.5	1	1.5	V

Protection delays

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Delay between short circuit and CSO1 high	$t_{DSCCSO1(H)}$[5]	G = 100 V_{EN}=3.3V	0.2	6.5	13	µs
Delay between CSO1 high and INT = low	$t_{DCSO1(H)INT(L)}$[5]	G = 100 V_{EN}=3.3V	0.5	5	10	µs
Delay between CP high and INT	$t_{DCP(H)INT(L)}$	$V_{CP(REF)MIN} \le V_{CP(REF)} \le V_{CP(REF)MAX}$	1	9	30	µs
Delay between UV on VS and INT = low	$t_{DUV(H)INT(L)}$	–	8	22	40	µs
Delay between INT = low and gate 80%	$t_{DINT(L)G(L)}$[6]	$C_{G(EQ)}$ = 100 nF	–	3	5	µs
Delay between short circuit and gate 80%	$t_{DSCG(L)}$[5]	G = 100 V_{EN}=3.3V $C_{G(EQ)}$ = 100 nF	0.7	16	24	µs
Time to reset	t_{RESET}	Reset from SAFESTATE: $V_{EN} < V_{EN(L)}$ for t_{RESET} duration	3	–	30	µs

Driver outputs

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power on input delay	t_{POI}	Time to activate protections before turn-on after INx = high	0	2	6.5	µs
Turn-on delay	$t_{D(ON)}$	$C_{G(EQ)}$ = 100 nF	1	4	7	µs
Rise time on gate 20% to 80% of V_{BC} - V_S	t_R	$C_{G(EQ)}$ = 100 nF	0	7	15	µs
Gate turn on short circuit pulsed current per gate	$I_{G(ON)}$	V_{GX} - V_{SX} = 0 V	50	175	250	mA
Turn-off delay	$t_{D(OFF)}$	$C_{G(EQ)}$ = 100 nF	1	4	7	µs
Fall time on gate 80% to 20% of VBC - VS	t_F	$C_{G(EQ)}$ = 100 nF	0	2	5	µs
Gate turn-off short circuit pulsed current per gate	$I_{G(OFF)}$	V_{GX} - V_{SX} = 14 V	350	1400	2000	mA

Boost converter (BC)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
BC Boost capacitor	C_{BC}[2]	$C_{G(EQ)}$ = external MOSFET equivalent gate source capacitance	20 * $C_{G(EQ)}$	–	–	F

BC switching current limitative resistor	R_{RS}[2]	Use 1/2 W resistor min.	10	–	30	Ω
BC output VBC - VS regulation voltage	$V_{BC(TH)}$	–	11.5	12.5	14	V
VBC(TH) to UVLO regulation gap	$V_{BC(RG)}$	–	1.9	2.5	–	V
BC undervoltage lockout voltage	*UVLO*	–	9.5	10	11	V
Delay between UVLO and INT=low	$t_{DUVLO(H)INT(L)}$	–	0	10	40	µs
RS deactivation threshold	$V_{RS(TH)}$	–	0.6	1	1.4	V
Forward voltage of BC diode	V_{FBC}	I_F = 100 mA	0	0.9	1.1	V
On-state resistance of BC switch	$R_{DS(ON)K1(25)}$	I = 100 mA; T_J = 25°C	1	11	15	Ω
Boost converter off-time	$t_{BC(OFF)}$	–	1	4	6	µs
Time to reach RS deactivation threshold	$t_{RS(TH)}$[4]	V_S = 48 V; R_{RS} = 10 Ω; L = 100 µH / 1.7 Ω; T_J = 25°C	–	920	–	ns
Turn-off delay of K1	$t_{D(OFF)K1}$	–	0.05	0.2	0.35	µs
Boost power-on delay	t_{pod}[3]	V_S = 48 V; R_{RS} = 10 Ω; L = 100 µH / 2 Ω ; C_{BC} = 1µF; T_J = 25°C	–	200	–	µs

Current consumption

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GND pin current in SLEEP mode	$I_{GND+RS(SLEEP)}$	V_S = 48 V V_{BC} = V_S	1	8	20	µA
Sources leakage current in SLEEP mode	$I_{SX(SLEEP)}$	V_{BAT} = 48 V V_S - V_{SX} = V_{BAT}	0.1	1	4	µA
VS pin current in IDLE mode	$I_{VS(IDLE)}$	V_S = 48 V V_{SX} = V_S	-25	-10	-3	µA
VS pin current in IDLE mode, 25°C	$I_{VS(IDLE)25}$	T_J = 25°C	-20	-10	-3	µA
BC current in IDLE mode	$I_{BC(IDLE)}$	V_S = 48 V V_{BC}-V_S = 14 V	10	15	80	µA
BC current in IDLE mode, 25°C	$I_{BC(IDLE)25}$	T_J = 25°C	10	15	40	µA
VS pin current in ON mode	$I_{VS(ON)}$	–	-40	-8	0	µA
VS pin current in ON mode, 25°C	$I_{VS(ON)25}$	T_J = 25°C	-20	-8	-2	µA
BC current in ON mode	$I_{BC(ON)}$	V_{BC} - V_S = 14 V	10	65	175	µA
BC current in ON mode, 25°C	$I_{BC(ON)25}$	T_J = 25°C	10	65	110	µA
BC current in ON mode, 25°C, one CSA disconnected	$I_{BC(ON)25\_1CSA(OFF)}$[2]	T_J = 25°C CSA 1 or 2 not used	10	45	75	µA
BC current in ON mode, 25°C, all amplifiers disconnected	$I_{BC(ON)25\_2CSA(OFF)}$[2]	T_J = 25°C CSA 1 and 2 not used	6	30	60	µA
BC current in ON mode, ≤ 85°C, one CSA disconnected	$I_{BC(ON)≤85\_1CSA(OFF)}$[2]	T_J ≤ 85°C CSA 1 or 2 not used	10	45	100	µA
BC current in ON mode,≤ 85°C, all amplifiers disconnected	$I_{BC(ON)≤85\_2CSA(OFF)}$[2]	T_J ≤ 85°C CSA 1 and 2 not used	6	30	75	µA
VS pin current in SAFESTATE mode	$I_{VS(SAFESTATE)}$	–	-40	-8	0	µA
BC current in SAFESTATE mode	$I_{BC(SAFESTATE)}$	V_{BC} - V_S = 14 V	10	65	175	µA

Note7：

1) Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

2) Not subject to production test, specified by design

3) Not subject to production test, specified by characterization.

4) Not subject to production test, specified by calculation.

5) Sum of $t_{DSCCSO1(H)}$, $t_{DCSO1(H)INT(L)}$,$t_{DINT(L)G(L)}$ max. does match max.

6) Of the sum $t_{DSCG(L)}$ due to silicon process and variation.

General operation

Operating modes

WS2510AT works with 4 operating modes: SLEEP, IDLE, ON and SAFESTATE, selected by a combination of inputs INA, INB and EN pins, and in the case of SAFESTATE, by protection features or force signal.

Table 2. Inputs, modes and outputs states

INPUTS			Operating mode		OUTPUTS								comments
EN	INA	INB			Boost converter output V_{BC} - V_S	INT	DG0	DG1	V_{CSO1}	V_{CSO2}	V_{TMPO}	V_{GA}-V_{SA}	V_{GB}-V_{SB}	
0	X	X	**SLEEP**		0	1*	0	0	0	0	0	0	0	*once reset is done, provided that pull-up voltage is available
1	0	0	**IDLE**		$V_{BC(TH)}$	1	0	0	0	0	0	0	0	
1	1	0	**ON**		$V_{BC(TH)}$	1	pulse when K1 activated*	direction of current CSA1*	active	active	active	$V_{BC(TH)}$	0	*high level: see V_{DG0}, V_{DG1} in Functional ranges Table
	0	1										0	$V_{BC(TH)}$	
	1	1										$V_{BC(TH)}$	$V_{BC(TH)}$	
1	X	X	**SAFESTATE**	SC or UV	$V_{BC(TH)}$	0	0	1	active	active	active	0	0	NB: if several faults occurs in series, only first fault is indicated by DG1 and DG0 *depends on UVLO root cause
				UVLO	≤ $V_{BC(TH)}$*		1	0						
				CP	$V_{BC(TH)}$		1	1						

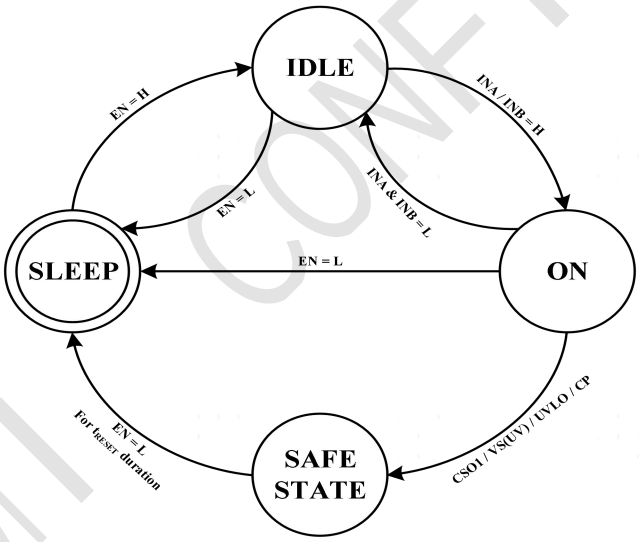
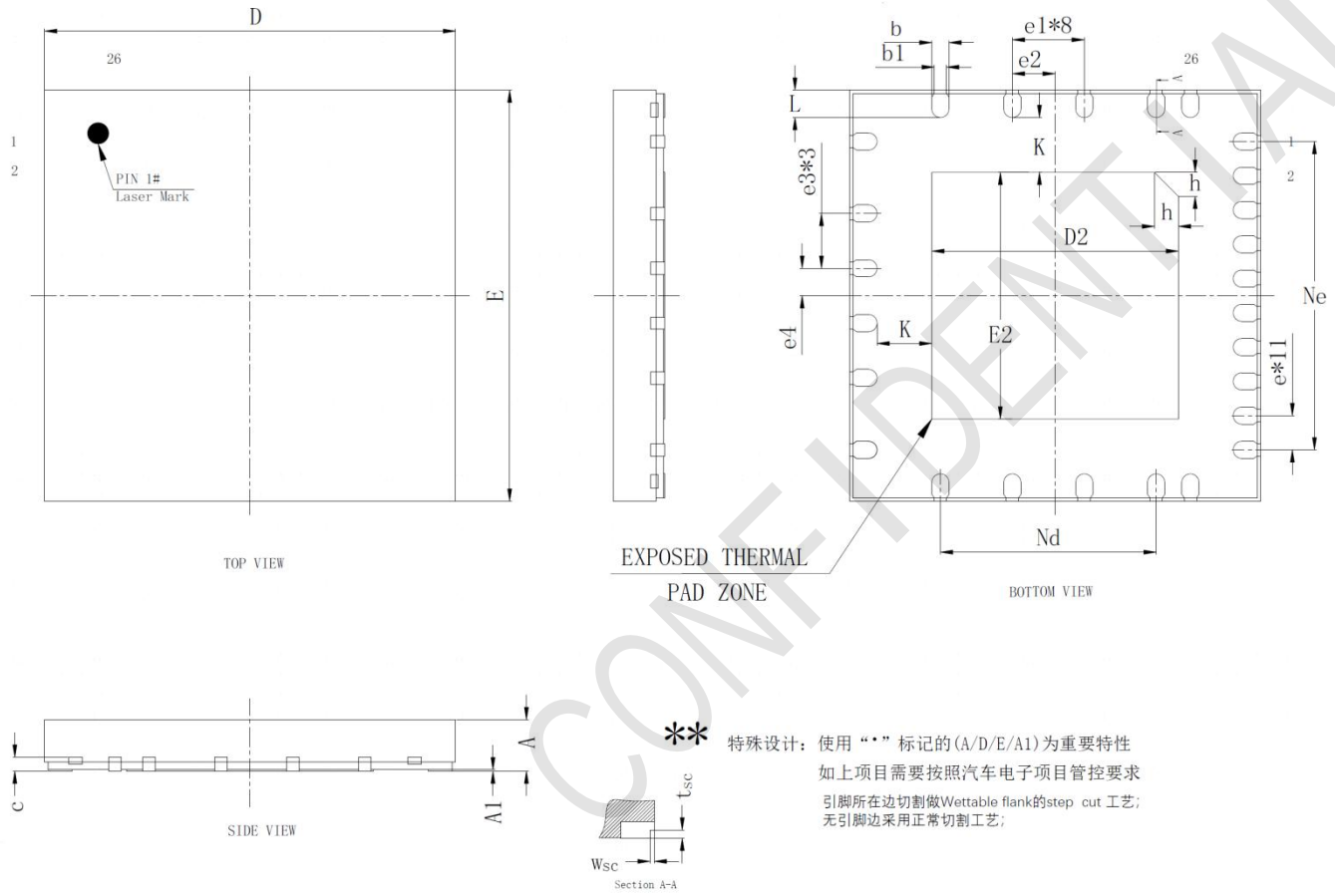


Figure 1. State machine

Package Outline

QFN6×6-26



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.2	0.25	0.3
b1		0.18REF	
c		0.203REF	
D	5.9	6	6.1
D2	3.5	3.6	3.7
e		0.5BSC	
e1		1.05BSC	
e2		0.625BSC	
e3		0.8BSC	
e4		0.4BSC	
Nd		3.15BSC	
E	5.9	6	6.1
E2	3.5	3.6	3.7
Ne		4.5BSC	
L	0.35	0.4	0.45
h	0.3	0.35	0.4
K		0.8REF	
W_{SC}	0.01		0.09
t_{SC}	0.08		0.18

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