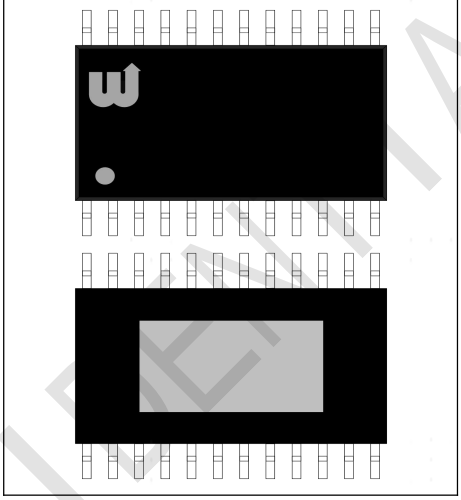
Application

- Fail operational power supply targeting high current applications
- Connection/isolation switch between power supplies (e.g. for hybrids and electric vehicles)
- Developed to support dependable power supply and distribution

Package	eTSSOP24L
Marking	WS2410AT



Basic Features

- AEC-Q100 qualified
- ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- One channel device with two high-side gate driver outputs
- 3 Ω pull-down, 50 Ω pull-up for fast switch on/off
- Support back-to-back MOSFET topologies (common drain and common source)
- Two bidirectional high-side analog current sense interfaces with externally adjustable gain
- Adjustable overcurrent/short-circuit protection
- Versatile comparator to implement: adjustable I-t wire protection, overvoltage/undervoltage or overtemperature protection

AEC Qualified

ISO 26262 ready

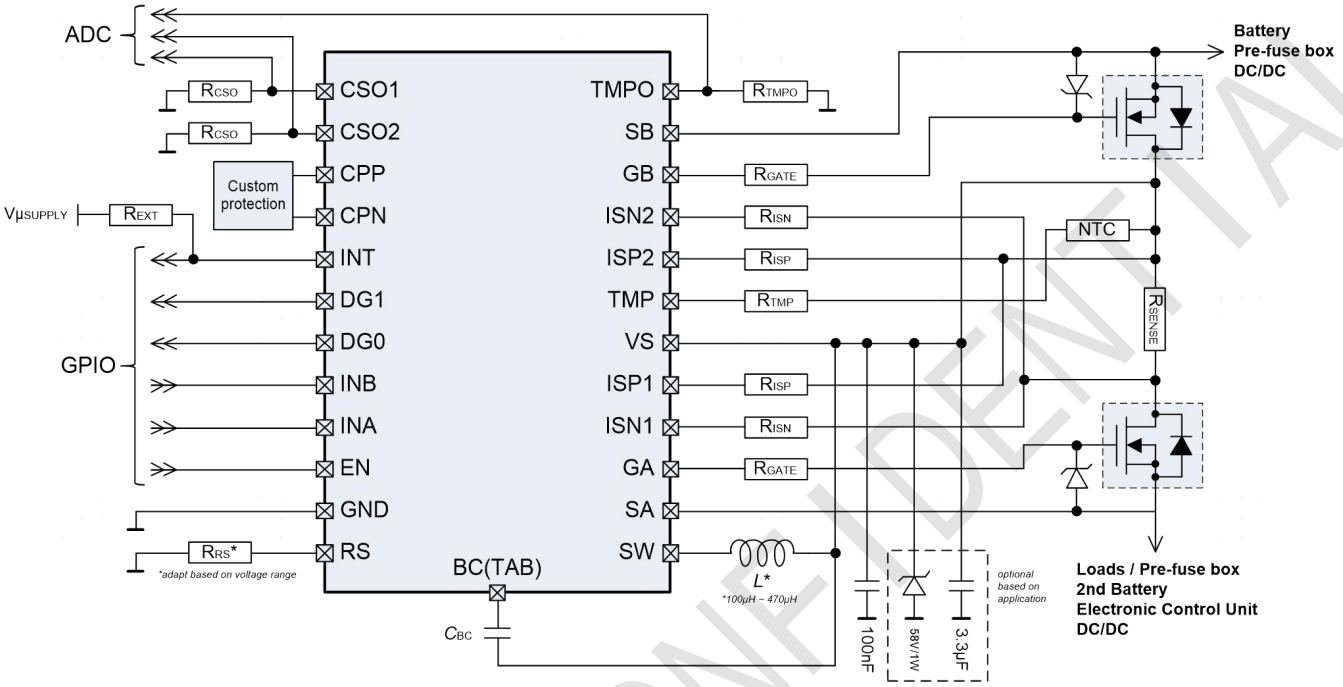
RoHS

Halogen-free

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_S	58V
Voltage reference range for normal operation	$V_{S(NOR)}$	8-36V
Voltage reference extended range	$V_{S(EXT)}$	3-58V
CSA adjustable gain	G	10~200
Gate turn on short circuit pulsed current per gate	$I_{G(ON)}$	175mA
Gate turn-off short circuit pulsed current per gate	$I_{G(OFF)}$	1400mA
Turn on delay	$t_{D(ON)}$	4us @ C_G=100nF
Turn off delay	$t_{D(OFF)}$	4us @ C_G=100nF
GND current in SLEEP mode	$I_{GND+RS(SLEEP)}$	1~15uA
BC current in IDLE mode	$I_{BC(IDLE)}$	5~50uA

Typical Application Circuit

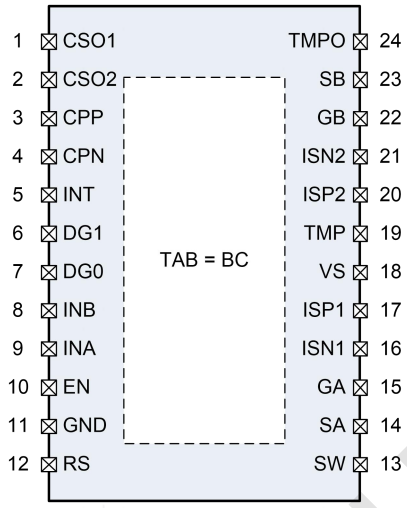


Ordering Information

Package	Top Mark	Part No.
eTSSOP24L, Pb-free	WS2410AT XXYMXX	WS2410AT

Pin Configuration

Top view



Pin Description

Pin Name	Pin NO.	Pin Description
CSO1	1	Analog voltage to force SAFESTATE mode. **C**urrent **S**ense **O**utput **1**: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP1/ISN1.
CSO2	2	**C**urrent **S**ense **O**utput **2**: analog voltage feedback, provides a voltage proportional to the shunt current or VDS across ISP2/ISN2.
CPP	3	**Comp**arator **P**ositive: analog positive input of comparator.
CPN	4	**Comp**arator **N**egative: analog negative input of comparator.
INT	5	**Int**errupt: open drain interrupt output.
DG1	6	**Diag**nostic **1**: DG1 is logic low in SLEEP mode and IDLE mode. Digital voltage information of current flow direction in ON mode: • DG1 is logic high if current flows from ISP1 to ISN1 connection • DG1 is logic low if current flows from ISN1 to ISP1 connection Digital voltage information in SAFESTATE mode: • DG1 is logic high if SAFESTATE because of CP or SC or VS(UV) • DG1 is logic low if SAFESTATE because of UVLO
DG0	7	**Diag**nostic **0**: DG0 is logic low in SLEEP mode and IDLE mode. Digital voltage information of boost converter frequency in ON mode. Digital information in SAFESTATE mode: • DG0 is logic high if SAFESTATE because of CP or UVLO • DG0 is logic low if SAFESTATE because of SC or VS(UV)

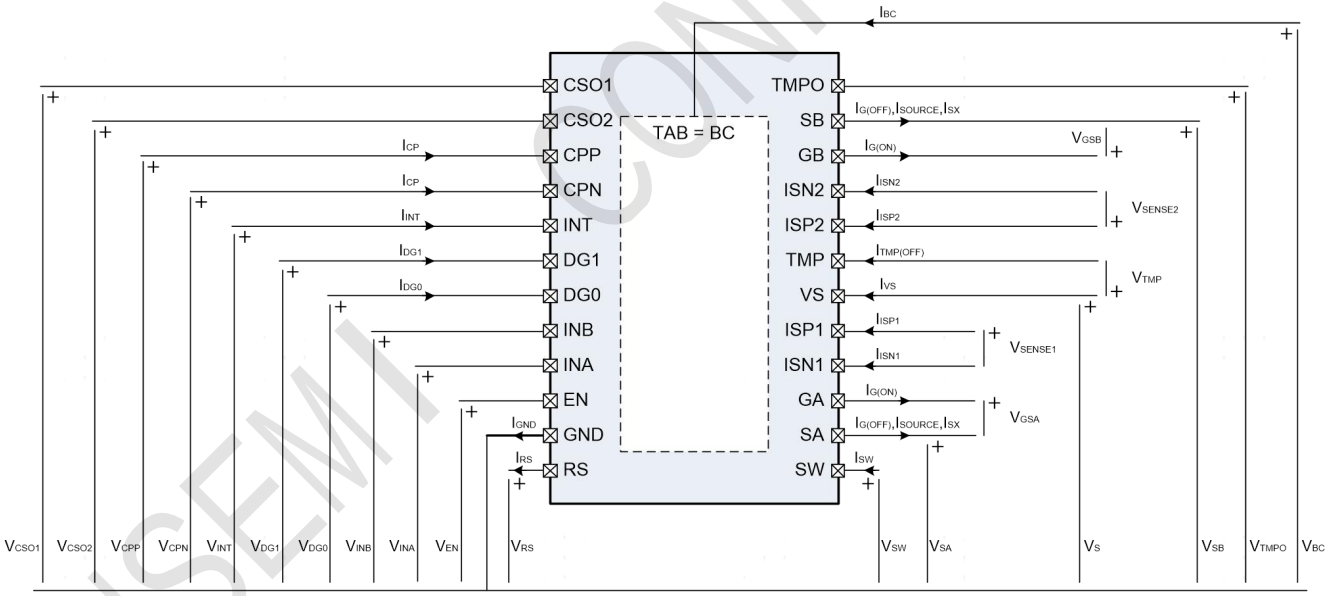
Pin Name	Pin NO.	Pin Description
INB	8	**In**put **B**: If INB digital logic is low, channel B switches OFF. If INB digital logic is high, channel B switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
INA	9	**In**put **A**: If INA digital logic is low, channel A switches OFF. If INA digital logic is high, channel A switches ON and gate driver is in ON mode only if pin ENABLE is logic high.
EN	10	**EN**ABLE: If EN digital logic is low, gate driver is in SLEEP mode, channels A and B are switched OFF and gate driver is RESET. If EN digital logic is high, gate driver is in IDLE mode when INA and INB are both logic low.
GND	11	**Grou**nd connection.
RS	12	**R**esistor **s**ense output of boost converter: current measurement of the boost converter.
SW	13	Switching supply input of boost converter. Inductance connection.
SA	14	**S**ource **A**: output A connection to external MOSFET sources.
GA	15	**G**ate **A**: output A connection to external MOSFET gates.
ISN1	16	**I S**ense **N**egative **1**: external shunt or VDS negative connection.
ISP1	17	**I S**ense **P**ositive **1**: external shunt or VDS positive connection.
VS	18	**V**oltage reference, extended 3 V to 58 V.
TMP	19	**Tem**perature Input: analog connection to external NTC or PTC thermistor.
ISP2	20	**I S**ense **P**ositive 2: external shunt or VDS negative connection.
ISN2	21	**I S**ense **N**egative 2: external shunt or VDS positive connection.
GB	22	**G**ate **B**: output B connection to external MOSFET gates.
SB	23	**S**ource **B**: output B connection to external MOSFET sources.
TMPO	24	**Tem**perature **O**utput: analog voltage feedback provides a voltage proportional to thermistor temperature.
BC	TAB	**B**oost **C**onverter output capacitor connection; driver supply.

Table 1. Suggested connections for unused and not connected pins

Pin Name	Pin NO.	How to connect pin to disable corresponding function
CSO1	1	GND (FLOAT can trigger random latch on CSO1 internal comparator)
CSO2	2	GND
CPP	3	GND (FLOAT can trigger random latch CPP)
CPN	4	EN (VS induces 'large' current consumption. GND can trigger random latch)
INT	5	FLOAT
DG1	6	FLOAT
DG0	7	FLOAT
INB	8	GND (FLOAT potential IBC increase, DPI sensitivity increased if SB GB floating, no IDLE mode)
INA	9	GND (FLOAT potential IBC increase, DPI sensitivity increased if SA GA floating, no IDLE mode)
EN	10	5V (@GND driver will always remain in SLEEP mode. EN can also be connected to VS with 100k+diode so driver is by default in IDLE mode as long as a power supply is connected > Vzener+Vrev_diode is present on VS pin. diode: cathode on VS.)
GND	11	GND (never leave open: can randomly activate boost converter, IC destruction))
RS	12	FLOAT (when using external supply directly on BC, RS connection to GND could cause IC destruction)
SW	13	FLOAT (in case of boost supply converter disconnection and driver external supply directly on BC)

Pin Name	Pin NO.	How to connect pin to disable corresponding function
SA	14	FLOAT (if GA not used)
GA	15	FLOAT
ISN1	16	GND/VS
ISP1	17	VS/GND
VS	18	VS (FLOAT: BC is not regulated, external MOSFET gate destruction expected).
TMP	19	FLOAT
ISP2	20	GND/VS
ISN2	21	VS/GND
GB	22	FLOAT
SB	23	FLOAT (if GB not used)
TMPO	24	FLOAT or GND
BC	TAB	Boost capacitor C_{BC} or external supply (see datasheet for V_{BC}-V_S functional range.

Current and Voltage Conventions



Note1：

1) Voltages are defined positive with respect to ground.

2) Currents are defined flowing into or from the pin depending on pins.

Absolute Maximum Ratings (Note2)

Symbol	Parameter	Value	Unit
V_{BC} - X	Maximum voltage V_{BC} (boost converter output) - all pins	-0.3 to 75	V
V_S - V_{SX}	Maximum drain-source voltages on each output	-36 to 75	V
V_{GX} - V_{SX}	Maximum voltage between gate and source pins on each output	-0.3 to 75	V
V_{SW} - V_{RS}	Maximum voltage between SW and RS pin	-0.3 to 75	V
I_{SW}	Maximum pulsed current in SW pin	200	mA
$T_{J(MAX)}$	Maximum operating junction temperature	-40 to 150	℃
$T_{STG(MAX)}$	Storage temperature	-55 to 150	℃

Note2：

1) Not subject to production test - specified by design.

2) Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Functional Ranges (Note3)

-40°C < T_j < 150°C, all voltages with respect to ground, typical values are given for V_S = 14 V and T_J = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{S(NOR)}$	Voltage reference range for normal operation	8	-	36	V
$V_{S(EXT)}$[2)]	Voltage reference extended range	3	-	58	V
$V_{S(SC)LOW}$	Voltage reference range with lower short-circuit protection	3	-	8	V
V_{EN}, V_{INA}, V_{INB}	Input pins EN, INA, INB	0	-	5.5	V
V_{DG0}, V_{DG1}[3)]	Diagnostic pins DG0, DG1	0	-	k_{DG}*V_{EN}	V
V_{INT}	Interrupt pin INT	0	-	5.5	V
$V_{CP(REF)}$	Comparator reference voltage pins CPN, CPP	1	-	5.5	V
$V_{AMP(SAT)}$[4)]	Analog output pins saturation CSO 1&2, TMPO	4	4.6	5.5	V
G[5)]	Current sense amplifiers gain range	10	-	200	-
V_{BC}-V_S	Supply voltage range for amplifier operation	6	-	15	V
V_{BC}-V_{ISxx}	Amplifier input voltage range	6	-	15	V
$V_{ISxx-GND(TH)}$	Amplifier input voltage threshold for disconnection	0.2	0.7	1.5	V

Note3：

1) Not subject to production test - specified by design.

2) Parameter deviations possible

3)See k_{DG} parameter

4)V_S = $V_{S(NOR)}$

5)For G ≤ 30, use only R_{CSO} = 10 kΩ

Thermal Resistance (Note3)

Symbol	Parameter	Value	Unit
T_{JA}	Thermal Resistance Junction-to-Ambient	27	K/W

Note3：

1) Not subject to production test - specified by design.

2) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. T_A = 85°C. Device is loaded with 1 W power.

ESD Susceptibility (Note4)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 2)	ESD HBM susceptibility all pins	±2	kV
$V_{ESD(CDM)}$ 3)	ESD CDM susceptibility all pins	±500	V
$V_{ESD(CDM)}$ 4)	ESD CDM susceptibility corner pins (pins 1, 12, 13, 24)	±750	V

Note5：

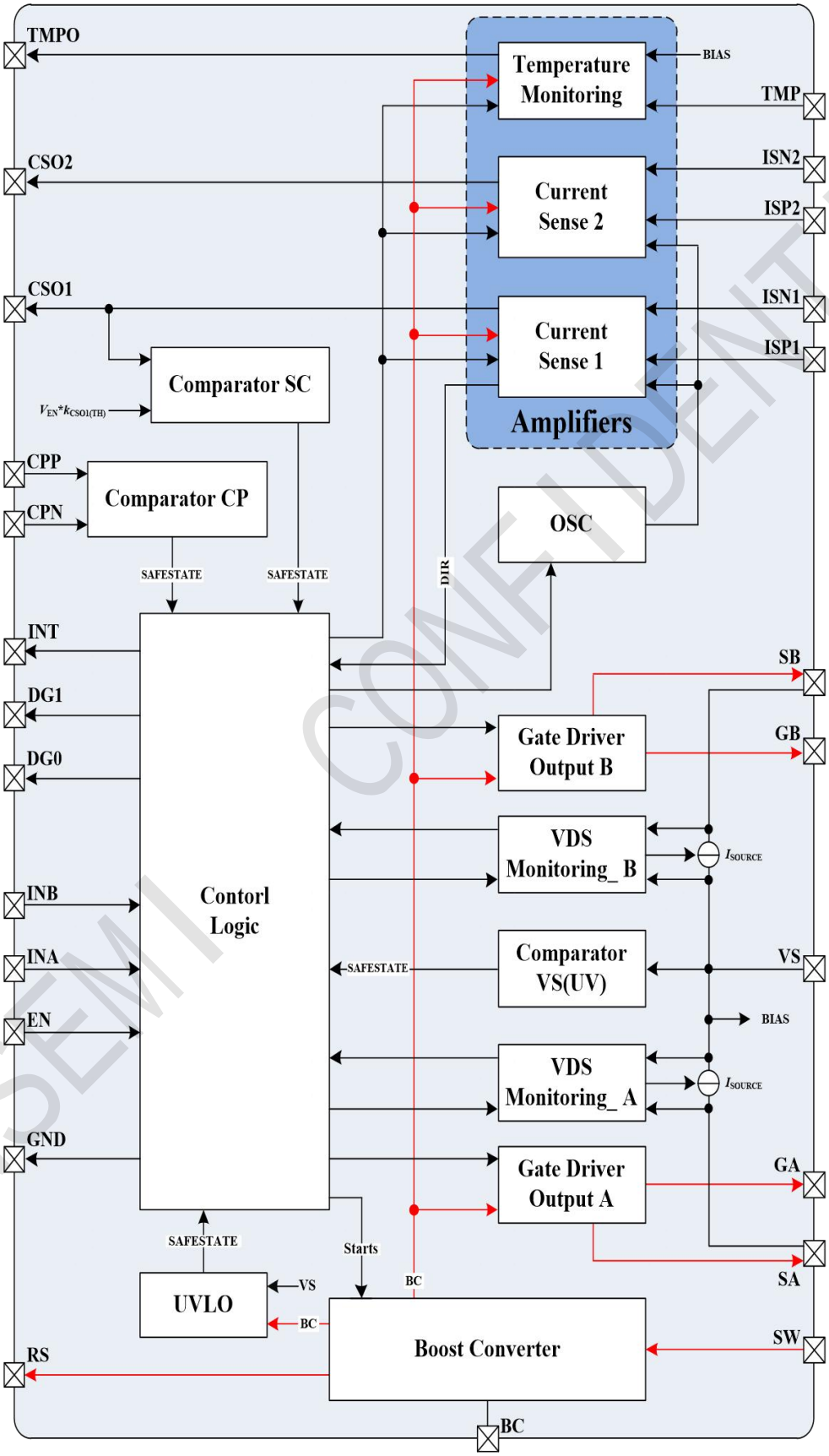
1) Not subject to production test - specified by design.

2) ESD susceptibility, Human Body Model “HBM”, according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

3) ESD susceptibility, Charged Device Model “CDM”, according to ANSI/ESDA/JEDEC JS-002.

4) ESD susceptibility, Charged Device Model “CDM”, according to ANSI/ESDA/JEDEC JS-002.

Functional Block



Electrical Characteristics (Note6)

T_J = -40 to 150°C, V_S = 8 V to 36 V (unless otherwise specified), all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), typical values are given for V_S = 14 V and T_J = 25°C

Inputs pins

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input A,B & Enable voltage high level	$V_{IN(H)}$, $V_{EN(H)}$	–	2.5	–	–	V
Input A,B & Enable voltage low level	$V_{IN(L)}$, $V_{EN(L)}$	–	–	–	0.7	V
Input A,B & Enable pull-down internal resistor	$R_{IN(GND)}$	–	0.5	1.5	2.5	MΩ
Input zener diode for local pins	$V_{Z(IN)}$ 2)	–	5	5.5	6	V

Digital diagnostic pins

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Ratio diagnostic pin voltage high level over V_{EN}	$k_{DG(H)}$	–	0.9	1	1.1	–
Diagnostic pin voltage low level	$V_{DG(L)}$	V_{BC} = 72 V	–	–	0.1	V
Diagnostic pin serial resistor	$R_{DG(GND)}$	–	5	10	20	kΩ
Delay for current direction change on DG1	t_{ISD}	Indicates current flow direction change on CSA1 only ON mode only	0	15	50	µs
Interrupt pin pull-down internal resistor, SAFESTATE active	R_{INT}	–	5	10	20	kΩ
Interrupt pin current leakage	$I_{INT(NOSAFESTATE)}$	$V_{INT(H)}$ ≤ 5.5 V	–	–	0.3	µA

Comparator (CP)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Comparator offset	$V_{CP(OFFSET)}$	$V_{CP(REF)MIN}$ ≤ $V_{CP(REF)}$ ≤$V_{CP(REF)MAX}$	-50	–	50	mV
Comparator leakage input current	I_{CP}	V_{CP} = 5.5 V	-100	–	500	nA

Temperature amplifier (TMPA)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
TMPA input current	$I_{TMP(OFF)}$	–	-100	–	100	nA
TMPA input offset	$V_{TMP(OFFSET)}$	–	-10	0	10	mV
TMPA ratio	k_{TMP}	–	9.5	10	10.5	–
TMPA pull-down resistor	R_{TMPO} 2)	–	20	–	100	kΩ

Current sense amplifiers (CSA1 & CSA2)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CSA input offset	$V_{ISx(OFFSET)}$ 2)	–	-50	0	50	µV
CSA input blind range	$V_{ISx(BLIND)}$	–	-500	0	500	µV
CSA delay maximum accuracy	$t_{CSA(ACC)}$	–	0	200	400	µs
CSA settling time	$t_{CSA(SET)}$ 2)	Step 25% , G=100	1	92	236	µs
CSA output pull-down resistor	R_{CSOx} 2)	–	10	20	50	kΩ

CSA gain intrinsic error	$\varepsilon_{(G)}$[2]	G = 10..200,Vsense>3mV	-1	0	1	%
CSA gain intrinsic error	$\varepsilon_{(G)}$[2]	G = 10..200,Vsense≤3mV	-5	0	5	%
PSRR - CSA power supply rejection ratio	$PSRR_{1kHz}$[3]	f = 1 kHz, G = 100,R_{CSO} = 20 kΩ，see Figure 34	–	105	–	dB
CMRR - CSA common mode rejection ratio	$CMRR_{1kHz}$[3]	f = 1 kHz, G = 100, R_{CSO} = 20 kΩ，see Figure 34	–	116	–	dB
Noise - CSA Voltage noise, RTI	$Noise$[3]	G = 100, R_{CSO} = 20 kΩ RTI	–	180	–	nV_{RMS}

Protection thresholds

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current shutdown internal threshold ratio from Enable pin voltage	$k_{CSO1(TH)}$	V_S = 8 V to 58 V ON mode, CSA1 only	0.71	0.74	0.77	–
Under voltage threshold	$V_{S(UV)}$	V_S - GND ON mode only	0.5	1	1.5	V

Protection delays

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Delay between short circuit and CSO1 high	$t_{DSCCSO1(H)}$[5]	G = 100 V_{EN}=3.3V	0.2	6.5	13	µs
Delay between CSO1 high and INT = low	$t_{DCSO1(H)INT(L)}$[5]	G = 100 V_{EN}=3.3V	0.5	5	10	µs
Delay between CP high and INT	$t_{DCP(H)INT(L)}$	$V_{CP(REF)MIN} \le V_{CP(REF)} \le V_{CP(REF)MAX}$	1	9	30	µs
Delay between UV on VS and INT = low	$t_{DUV(H)INT(L)}$	–	8	22	40	µs
Delay between INT = low and gate 80%	$t_{DINT(L)G(L)}$[6]	$C_{G(EQ)}$ = 100 nF	–	3	5	µs
Delay between short circuit and gate 80%	$t_{DSCG(L)}$[5]	G = 100 V_{EN}=3.3V $C_{G(EQ)}$ = 100 nF	0.7	16	24	µs
Time to reset	t_{RESET}	Reset from SAFESTATE: $V_{EN} < V_{EN(L)}$ for tRESET duration	3	–	30	µs

Driver outputs

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power on input delay	t_{POI}	Time to activate protections before turn-on after INx = high	0	2	6.5	µs
Turn-on delay	$t_{D(ON)}$	$C_{G(EQ)}$ = 100 nF	1	4	7	µs
Rise time on gate 20% to 80% of V_{BC} - V_S	t_R	$C_{G(EQ)}$ = 100 nF	0	7	15	µs
Gate turn on short circuit pulsed current per gate	$I_{G(ON)}$	V_{GX} - V_{SX} = 0 V	50	175	250	mA
Turn-off delay	$t_{D(OFF)}$	$C_{G(EQ)}$ = 100 nF	1	4	7	µs
Fall time on gate 80% to 20% of V_{BC} - V_S	t_F	$C_{G(EQ)}$ = 100 nF	0	2	5	µs
Gate turn-off short circuit pulsed current per gate	$I_{G(OFF)}$	V_{GX} - V_{SX} = 14 V	350	1400	2000	mA

Boost converter (BC)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
BC Boost capacitor	C_{BC} [2]	$C_{G(EQ)}$ = external MOSFET equivalent gate source capacitance	20 * $C_{G(EQ)}$	–	–	F
BC switching current limitative resistor	R_{RS} [2]	Use 1/2 W resistor min.	10	–	30	Ω
BC output VBC - VS regulation voltage	$V_{BC(TH)}$	–	11.5	12.5	14	V
VBC(TH) to UVLO regulation gap	$V_{BC(RG)}$	–	1.9	2.5	–	V
BC undervoltage lockout voltage	*UVLO*	–	9.5	10	11	V
Delay between UVLO and INT=low	$t_{DUVLO(H)INT(L)}$	–	0	10	40	µs
RS deactivation threshold	$V_{RS(TH)}$	–	0.6	1	1.4	V
Forward voltage of BC diode	V_{FBC}	I_F = 100 mA	0	0.9	1.1	V
On-state resistance of BC switch	$R_{DS(ON)K1(25)}$	I = 100 mA; T_J = 25°C	1	11	15	Ω
Boost converter off-time	$t_{BC(OFF)}$	–	1	4	6	µs
Time to reach RS deactivation threshold	$t_{RS(TH)}$ [4]	V_S = 12 V; R_{RS} = 10 Ω; L = 100 µH / 1.7 Ω; T_J = 25°C	–	920	–	ns
Turn-off delay of K1	$t_{D(OFF)K1}$	–	0.05	0.2	0.35	µs
Boost power-on delay	t_{pod} [3]	V_S = 12 V; R_{RS} = 10 Ω; L = 100 µH / 2 Ω ; C_{BC} = 1µF; T_J = 25°C	–	550	–	µs

Current consumption

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GND pin current in SLEEP mode	$I_{GND+RS(SLEEP)}$	V_S = 24 V; V_{BC} = V_S	1	6	15	µA
Sources leakage current in SLEEP mode	$I_{SX(SLEEP)}$	V_{BAT} = 24 V; V_S - V_{SX} = V_{BAT}	0.1	0.5	4	µA
VS pin current in IDLE mode	$I_{VS(IDLE)}$	V_S = 24 V; V_{SX} = V_S	-15	-6	-2	µA
VS pin current in IDLE mode, 25°C	$I_{VS(IDLE)25}$	T_J = 25°C	-10	-6	-2	µA
BC current in IDLE mode	$I_{BC(IDLE)}$	V_S = 24 V; V_{BC}-V_S = 14 V	5	15	50	µA
BC current in IDLE mode, 25°C	$I_{BC(IDLE)25}$	T_J = 25°C	5	15	20	µA
VS pin current in ON mode	$I_{VS(ON)}$	–	-20	-4	0	µA
VS pin current in ON mode, 25°C	$I_{VS(ON)25}$	T_J = 25°C	-10	-4	-1	µA
BC current in ON mode	$I_{BC(ON)}$	V_{BC} - V_S = 14 V	10	65	175	µA
BC current in ON mode, 25°C	$I_{BC(ON)25}$	T_J = 25°C	10	65	110	µA
BC current in ON mode, 25°C, one CSA disconnected	$I_{BC(ON)25\_1CSA(OFF)}$ [2]	1) T_J = 25°C CSA 1 or 2 not used	10	45	75	µA
BC current in ON mode, 25°C, all amplifiers disconnected	$I_{BC(ON)25\_2CSA(OFF)}$ [2]	1) T_J = 25°C CSA 1 and 2 not used	6	30	60	µA

BC current in ON mode, ≤ 85°C, one CSA disconnected	$I_{BC(ON)≤85\_1CSA(OFF)}$ 2)	1) T_J ≤ 85°C CSA 1 or 2 not used	10	45	100	µA
BC current in ON mode,≤ 85°C, all amplifiers disconnected	$I_{BC(ON)≤85\_2CSA(OFF)}$ 2)	1) T_J ≤ 85°C CSA 1 and 2 not used	6	30	75	µA
VS pin current in SAFESTATE mode	$I_{VS(SAFESTATE)}$	–	-20	-4	0	µA
BC current in SAFESTATE mode	$I_{BC(SAFESTATE)}$	V_{BC} - V_S = 14 V	10	65	175	µA

Note7：

1) Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

2) Not subject to production test, specified by design

3) Not subject to production test, specified by characterization.

4) Not subject to production test, specified by calculation.

5) Sum of tDSCCSO1(H), tDCSO1(H)INT(L),tDINT(L)G(L) max. does match max.

6) Of the sum tDSCG(L) due to silicon process and variation.

General operation

Operating modes

WS2410AT works with 4 operating modes: SLEEP, IDLE, ON and SAFESTATE, selected by a combination of inputs INA, INB and EN pins, and in the case of SAFESTATE, by protection features or force signal.

Table 2. Inputs, modes and outputs states

INPUTS			Operating mode		OUTPUTS								comments
EN	INA	INB			Boost converter output V_{BC} - V_S	INT	DG0	DG1	V_{CSO1}	V_{CSO2}	V_{TMPO}	V_{GA}-V_{SA}	V_{GB}-V_{SB}	
0	X	X	**SLEEP**		0	1*	0	0	0	0	0	0	0	*once reset is done, provided that pull-up voltage is available
1	0	0	**IDLE**		$V_{BC(TH)}$	1	0	0	0	0	0	0	0	
1	1	0	**ON**		$V_{BC(TH)}$	1	pulse when K1 activated*	direction of current CSA1*	active	active	active	$V_{BC(TH)}$	0	*high level: see V_{DG0}, V_{DG1} in Functional ranges Table
	0	1										0	$V_{BC(TH)}$	
	1	1										$V_{BC(TH)}$	$V_{BC(TH)}$	
1	X	X	**SAFESTATE**	SC or UV	$V_{BC(TH)}$	0	0	1	active	active	active	0	0	NB: if several faults occurs in series, only first fault is indicated by DG1 and DG0 *depends on UVLO root cause
				UVLO	≤ $V_{BC(TH)}$*		1	0						
				CP	$V_{BC(TH)}$		1	1						

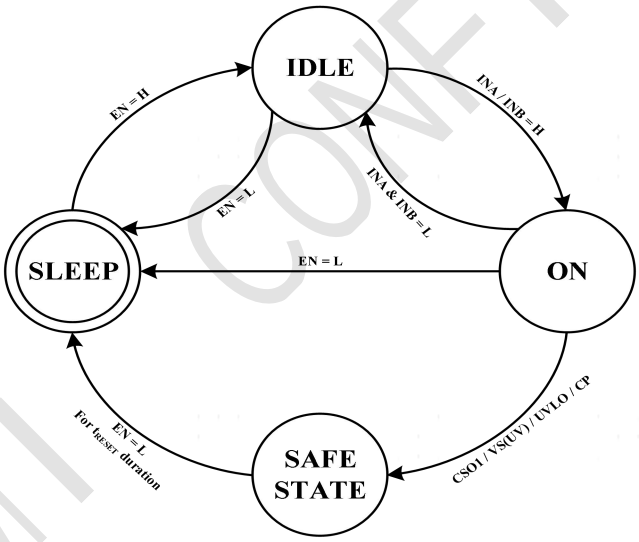


Figure 1. State machine

Current consumption

The current consumption of the driver from the system battery(or power supply), also named quiescent current (Iq) of WS2410AT, depends on:

- the mode the driver is in.
- the external components used for the boost converter, which is both the driver supply and the external MOSFET gate supply.
- for SLEEP mode, it also depends on the MOSFET structure used.

In this datasheet are only given consumption at d

river level, not at system battery/power supply level.

Details of quiescent current calculation from the battery are given in the application note "Getting started with WS2410AT".

Timing diagram

The following diagram shows digital inputs, digital outputs, the boost converter output and gate outputs from SLEEP to ON until short-circuit event occurs, and the reset procedure back to SLEEP mode.

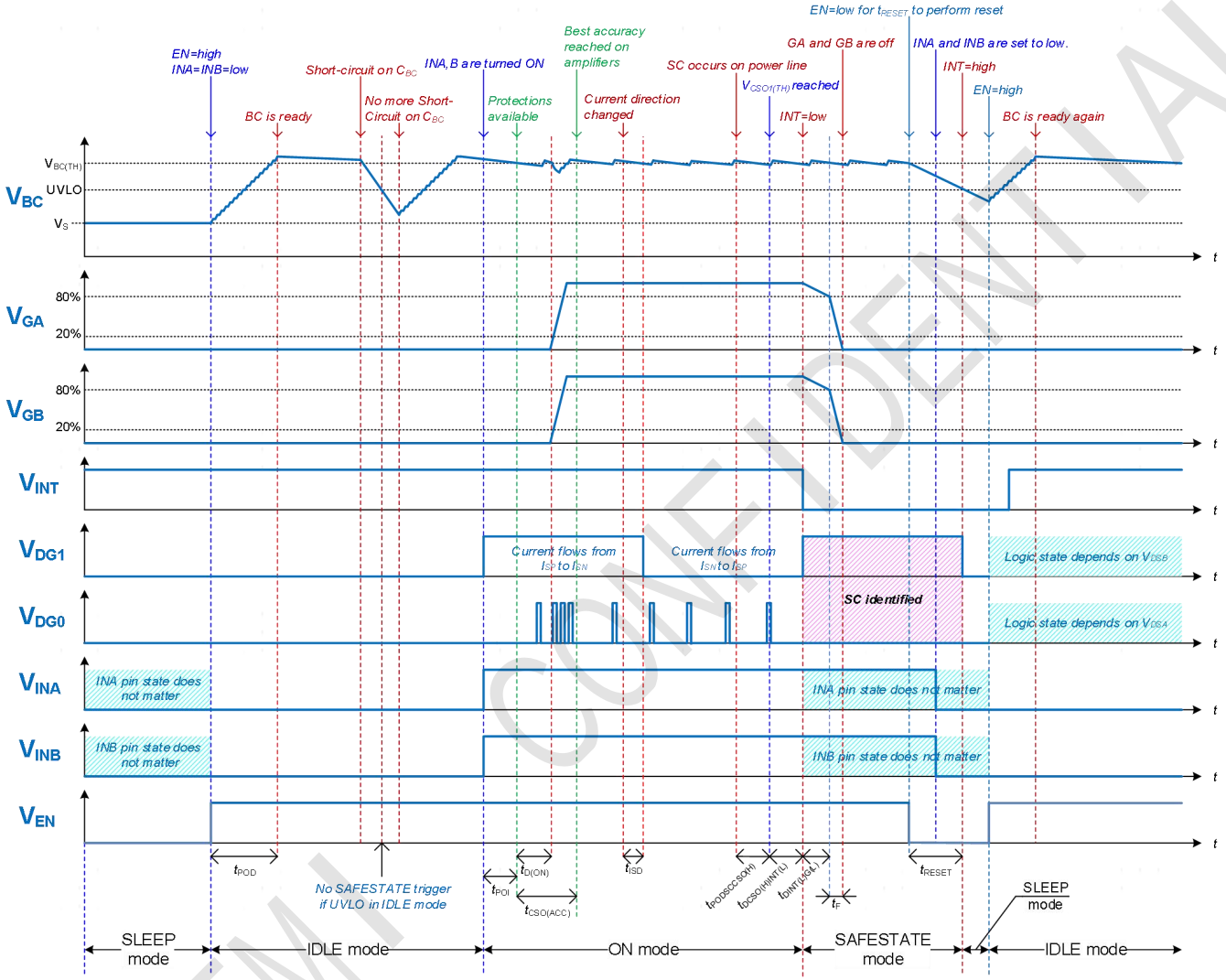


Figure 2. Timings diagram with IDLE mode, ON mode with short-circuit event and SAFESTATE with reset

- Note: time and voltages are not to scale

Logic pins

The following diagram shows digital inputs, digital outputs, the boost converter output and gate outputs from SLEEP to ON until short-circuit event occurs, and the reset procedure back to SLEEP mode.Logic pins are compatible to 5 V and 3.3 V microcontrollers. They can be connected directly to a microcontroller

output without the need of an additional component. There is an internal series and pull-down resistor($R_{IN(GND)}$) . A RC network for stabilizing voltage on EN pin can be used, since EN voltage is used for internal reference in the logic.

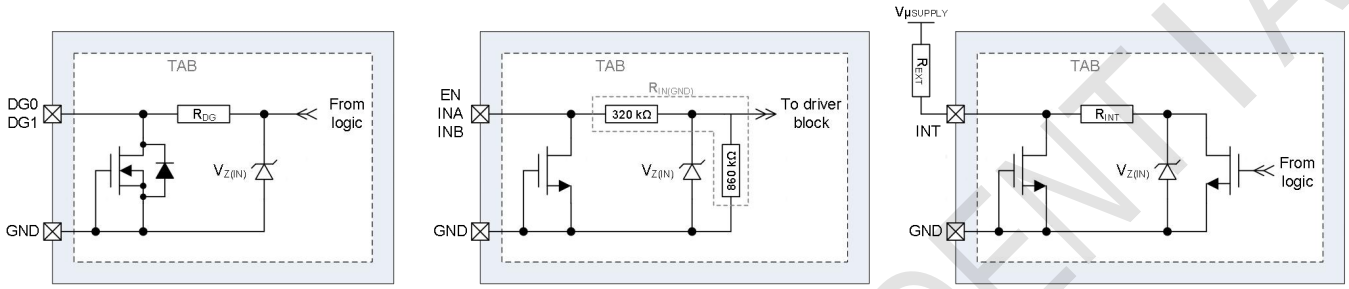


Figure 3. Digital I/O

The inputs control circuitry drives the output gate driver stage. They are pulled-down to GND with a $R_{IN(GND)}$ resistor to avoid unintended switch-on.

The inputs circuitry are set to logic high when $V_{INX} > V_{IN(H)}$ or $V_{EN} > V_{EN(H)}$.

The EN pin controls the ON/OFF of the boost converter and biases all analog logic.

EN = 1 sets V_{BC}-$V_S \geq V_{BC(TH)}$ after a time t_{POD}.

The INx pins directly control the gate outputs therefore INA = 1 sets GA = 1 and INB = 1 sets GB = 1. The inputs/outputs A and B are independent.

If EN and at least one of the INx pins are set high together, protections and measurements are turned ON but gates will turn-on only when V_{BC}-$V_S \geq V_{BC(TH)}$.

When driver enters ON mode by INx = 1, protections are ready after a time t_{POI} and amplifiers get maximum accuracy after a time $t_{CSA(ACC)}$).

The INx and EN pins are set to logic low when $V_{INX} < V_{IN(L)}$ or $V_{EN} < V_{EN(L)}$.

The digital outputs give back either a low or high logic level signal. The output high voltage level is based on V_{EN} and is given in the electrical characteristics table as a ratio between V_{DGx} and V_{EN}. See parameter k_{DG} in "Electrical Characteristics".

DG0 and DG1 in a low logic state have a value ≤ $V_{DG(L)}$. The state of the diagnostic depends the operating mode the driver is in, refer to "Operating modes".

In ON mode, DG0 reflects the activation of boost converter switch K1 (see "Driver supply: boost converter"): each time K1 is activated, DG0 = 1.

In ON mode, DG1 reflects the current direction on CSA1: DG1 = 0 if current is flowing from ISP1 to ISN1, DG1 = 1 if current is flowing from ISN1 to ISP1 (see "Measurement features").

INT pin is an open-drain output. The intent is to deliver an interrupt signal to relevant surrounding devices, such as microcontroller or power supply management chip.

INT needs to be externally pulled-up, e.g. to the microcontroller supply $V_{\mu SUPPLY}$. The value of V_{INT} when SAFESTATE is triggered, is the result of the voltage divider between the external resistor R_{EXT} and R_{INT}.

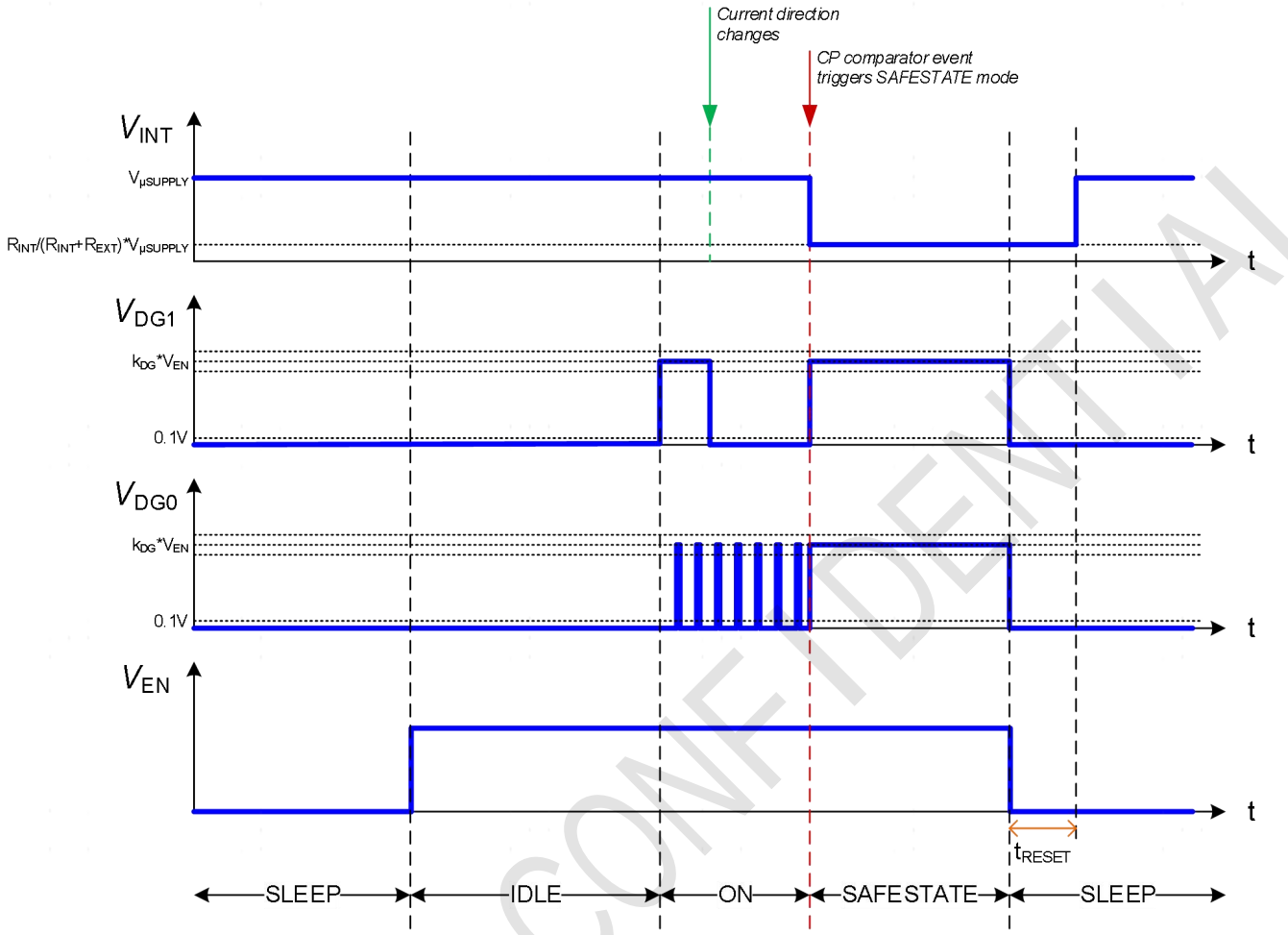


Figure 4. Diagnostics behavior

Gate outputs

WS2410AT features two identical gate outputs GA and GB working with source pins SA and SB respectively.

These outputs are activated by setting the corresponding digital input INA or INB to a high logic level.

The structure of these outputs is a push-pull and the logic ensures by design that both MOSFET K2x and K3x will not be ON at the same time (no shoot-through).

K2x are P-channel enhancement MOSFET and K3x are N-channel enhancement MOSFET.

The current to switch ON the external MOSFET connected to the gate driver is delivered by boost converter capacitor C_{BC}, through K2x to the gate pins Gx.

The current to switch OFF the external MOSFET is sunk from gate pins Gx through K3x to the source pins Sx.

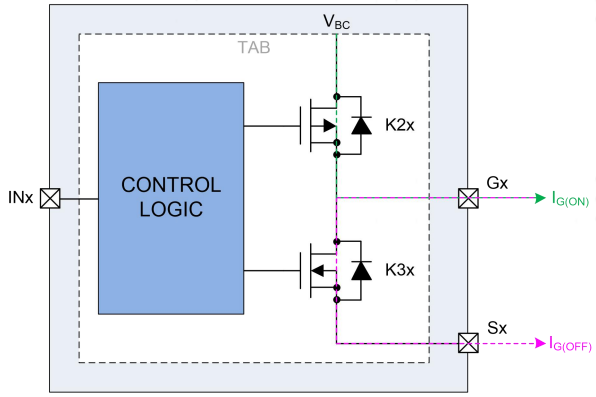


Figure 5. Gate output structure

When the first input is switched on, a time delay t_{POI} needs to be considered. This time delay, power-on-input, is needed to make sure protections are activated before sending gate signal activation, so WS2410AT never switches the MOSFET on without current sense and temperature amplifiers. If these functions are not used, t_{POI} still needs to be considered.

If V_{BC} - V_S ≤ $V_{BC(TH)}$ when the input signals INx are set high, the driver will be in ON mode but the gate outputs will remain OFF until $V_{BC(TH)}$ is reached on boost converter output.

If V_{BC} - V_S ≤ $V_{BC(TH)}$ occurs when the gates are ON, this under-voltage on the boost converter will trigger the lock-out of the gates and the driver will enter SAFESTATE, consequently turning and keeping off the gates. See "Gate undervoltage lock-out protection" and refer to "Driver supply: boost converter" to see how gate outputs and the boost converter are connected.

The timings for the gate outputs are described in Figure 6.

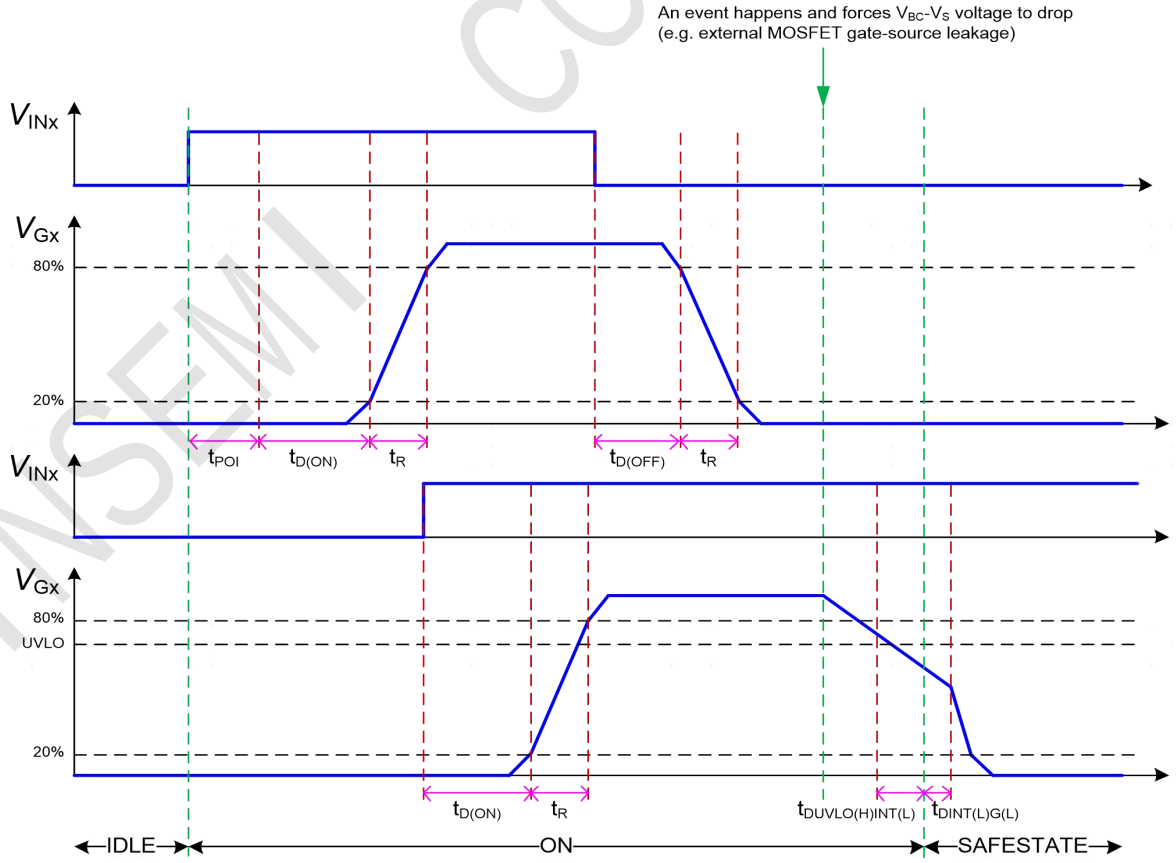


Figure 6. Gate timings (not to scale, for understanding purposes only)

Ground loss protection: module level

MOSFET K3 (see Figure 5, "Gate outputs") is turned on by default on each output as long as VS present.

If GND board/ECU connection is lost, K3 remains on or is turned on as long as the below conditions are true.

As a result gate-source is pulled-down in the following conditions:

- VS pin is connected to battery line
- GND board/ECU disconnected
- SLEEP, IDLE, ON or SAFESTATE modes

In ON mode, if GND board/ECU is connected back, driver outputs will be turned on again (and therefore K3 switch off) without necessary reset from pin ENABLE.

Current senses in ON and SAFESTATE modes

WS2410AT features two integrated current sense amplifiers (active in ON and SAFESTATE modes).

These **current sense amplifiers CSA1 and CSA2** are implemented with two identical differential amplifiers with a wide adjustable gain (G) .

The inputs are ISP1/2 and ISN1/2 pins and the outputs are CSO1/2 pin.

The current sensors must have a high-side position, or be positioned between the MOSFET drains in a back-to-back common drain configuration.

The current sense amplifier allows to monitor the currents flowing into the shunt (or MOSFET) in **both** directions, which is referred to as bidirectional current sensing.

The gain is set with external resistors $R_{ISP1/2}$ = $R_{ISN1/2}$ on input (on sensor side) and $R_{CSO1/2}$ on output (on microcontroller/connector side). R_{ISP} and R_{ISN} can be different if a different gain is necessary depending of the current direction. On CSA1, this difference in gain will also impact the short-circuit protection which can be higher or lower depending on the gain magnitude.

Resistor values can be adjusted based on the customer's current sensor solution.

The output is an analog voltage signal, $V_{CSO1/2}$, which represents the current flowing in the current sensor. It can be directly read on pin CSO1/2 (Current Sense Output) by a microcontroller. $V_{CSO1/2}$ output voltage varies from 0 V to V_{EN}, in both directions, allowing better accuracy than current sensors using an offset as middle point for zero current.

The information of current direction is available only for CSA1 and can be read in ON mode directly on pin DG1 (0 if current direction is from ISN1 to ISP1, 1 otherwise) by a microcontroller.

CSA1 features an integrated comparator for fast short-circuit protection. See "Short-circuit protection".

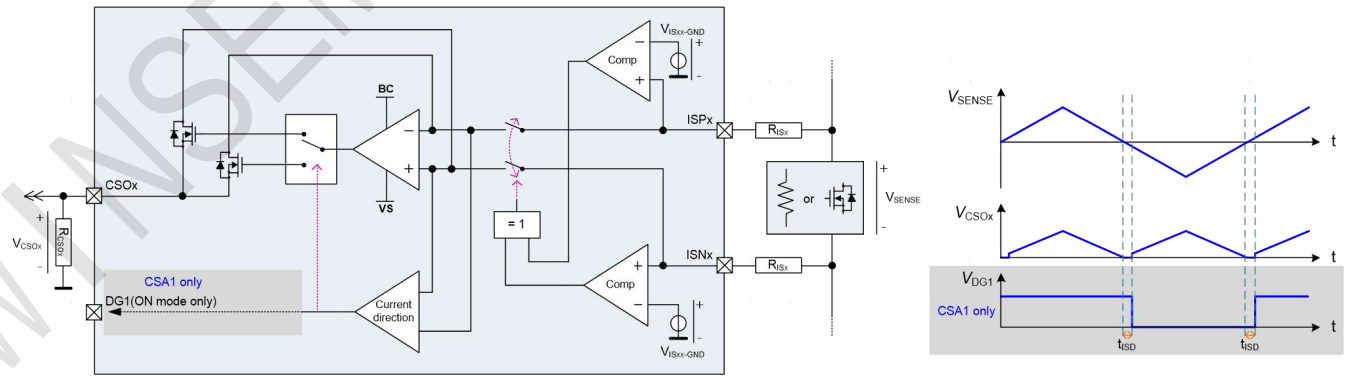


Figure 10. Current sense measurement principle and timing diagram [not to scale]

The amplifiers are supplied between BC and VS. If the V_{BC}-V_S voltage is below or above its functional range, the amplifiers input switches will open. As a result the current sense function is ensured and random reconnection can connect unwanted SAFESTATE.

The gain of the current sense amplifiers is configurable by three external resistors (R_{CSO}, 2 × R_{IS}).

The relationship between V_{SENSE} and V_{CSO} through the current sense amplifier is given by:

$$V_{CSO} = |V_{SENSE}| \frac{R_{CSO}}{R_{IS}} \quad (1)$$

Where the gain is set by:

$$G_{CSO} = \frac{R_{CSO}}{R_{IS}} \quad (2)$$

Special care has to be taken when setting the gain and the parameters G_{CSO} and R_{CSO} must be observed. Resistors are recommended with at least 1% precision and should be placed as close as possible to the WS2410AT pins. See application note "Getting started with WS2410AT" for a complete description on how to use the current sense amplifiers.

If not used, CSA1 or CSA2, or both, can be simply disconnected with the following configuration. One of the two input pins, either ISP or ISN needs to be connected close to GND (see $V_{ISxx-GND(TH)}$).

This will reduce the driver self-consumption in ON and SAFESTATE modes.

Warning: short-circuit protection with internal comparator on CSA1 will also be disabled if CSA1 is disabled.

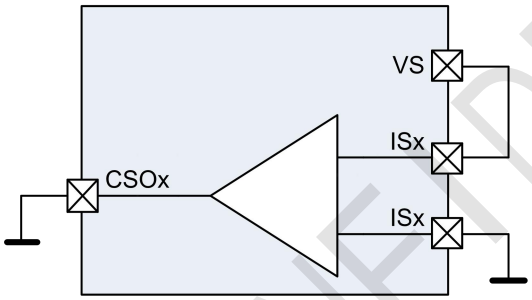


Figure 11. CSA1 & 2 disconnection configuration

Temperature measurement amplifier in ON and SAFESTATE modes

WS2410AT features an integrated temperature monitoring amplifier **TMPA** (active in ON and SAFESTATE modes).

This **temperature monitoring** function is implemented with a differential amplifier.

The input pin is TMP and the output pin is TMPO.

The temperature amplifier allows to monitor the heat flowing into the R_{NTC} by monitoring V_{TMPO} .

The gain is not directly adjustable and the ratio k_{TMP} is kept constant by the driver auto-adjusting the gain.

The ratio is kept with the R_{NTC} in input and R_{TMPO} in output. Resistor values can be adjusted based on customer's thermistor solution.

In the present document, the temperature sensor is referred to as "R_{NTC}" but other sensors, such as PTC or other thermistors can be implemented.

The output is an analog voltage signal: V_{TMPO} represents the temperature in the R_{NTC}. It can be directly read on pin TMPO (Temperature Output) by a microcontroller. R_{TMP} is not mandatory, but may be needed for linearisation of the output signal V_{TMPO}, depending on the thermistor solution choice.

Finally, TMPA can also be disabled if not used. TMP and TMPO pins can be left open.

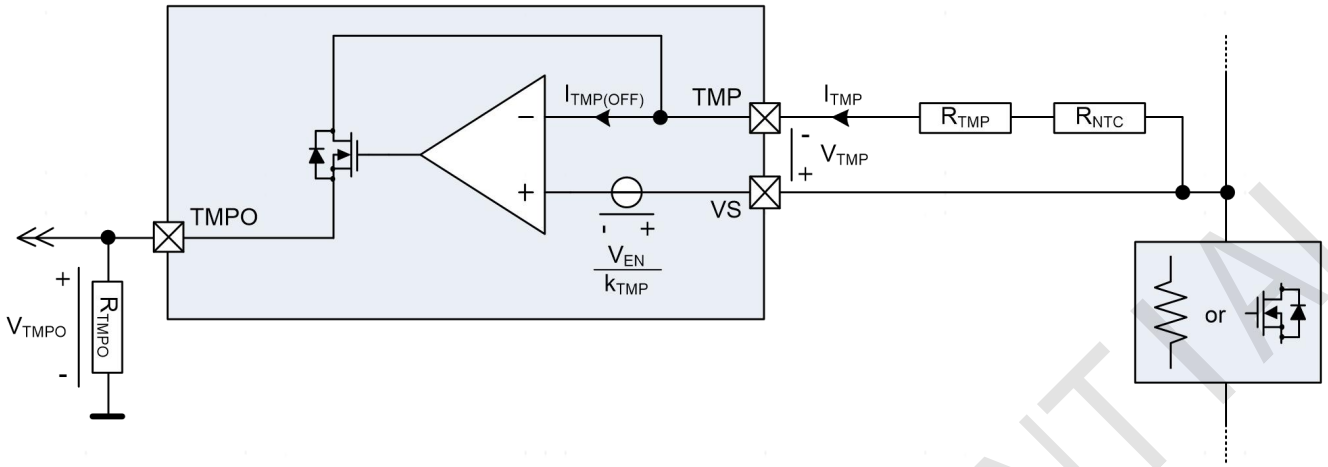


Figure 12. Temperature measurement diagram

The ratio k_{TMP} is defined as follows according to the Figure 12.

$$k_{TMP} = \frac{V_{EN}}{V_{TMP}} \quad (3)$$

Protections features in ON mode

Short-circuit protection

CSA1 has a fast comparator on its output CSO1, which allows WS2410AT to enter SAFESTATE mode when VCSO1 reaches $V_{CSO(TH)}$ = k_{CSO} x V_{EN}.

This allows fast turn-off delay time in case of overcurrent/short-circuit when CSA1 is used. WS2410AT is able to switch off the MOSFET without the microcontroller.

The turn-off delay time is $t_{DSCG(L)}$ and can be computed by the sum $t_{DSCCSO1(H)}$ + $t_{DCSO1(H)INT(L)}$ + $t_{DINT(L)G(L)}$. However, the maximum of $t_{DSCG(L)}$ is not the sum of the maximum of the other delays, because by construction, the silicon process and variation make such a case impossible. This is why only the maximum of $t_{DSCG(L)}$ should be considered when considering the worst case turn-off delay in case of short-circuit detection by CSA1 comparator.

See "Operating modes" for details on diagnostics in SAFESTATE mode.

Once in SAFESTATE mode, the driver needs to be reset.

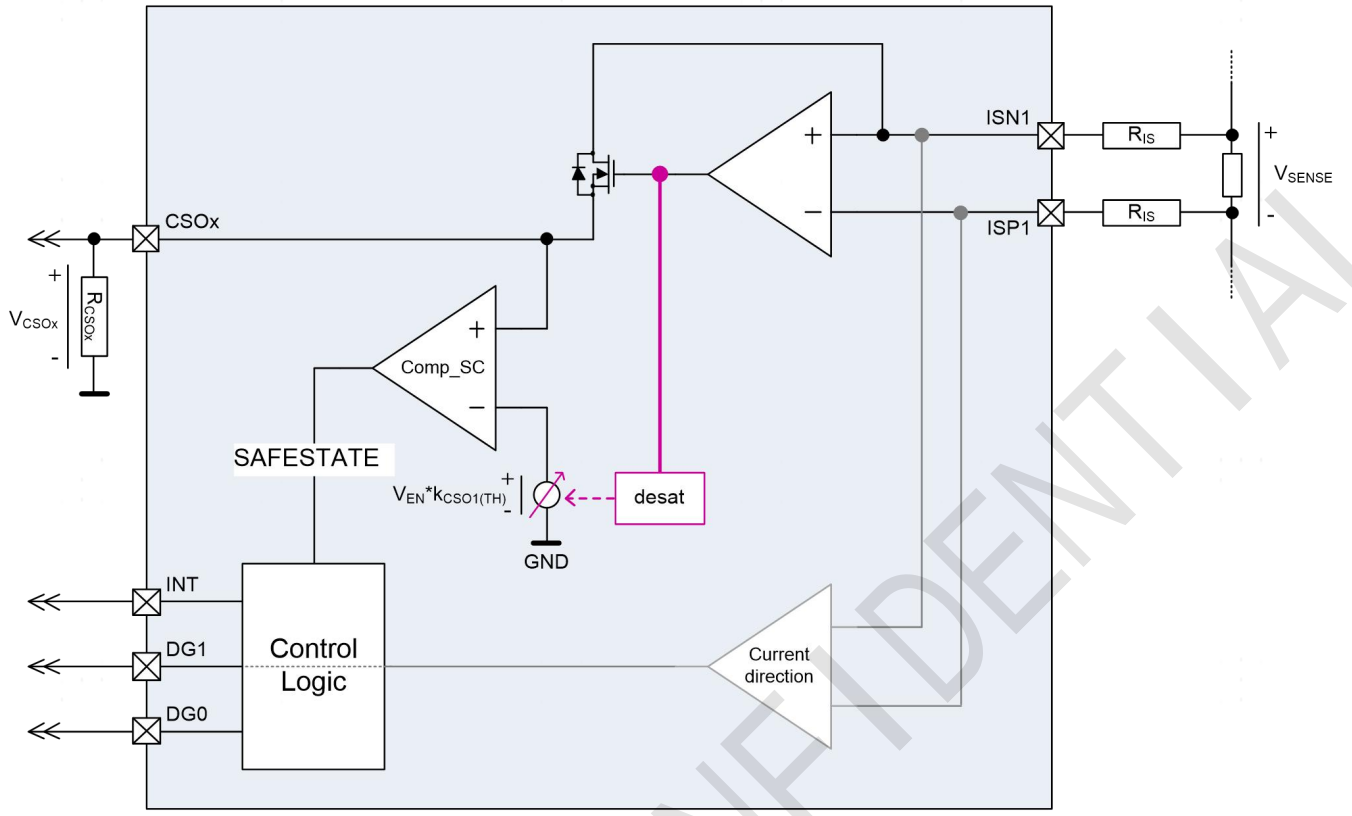


Figure 13. CSA1, internal comparator and diagnostics (one amplifier direction represented for simplicity)

The nominal voltage range for short-circuit protection is $V_{S(NOR)}$. As represented in the graph in Figure 14, in the $V_{S(SC)LOW}$ range, WS2410AT keeps operating if already in ON or IDLE mode. In the $V_{S(SC)LOW}$ range the short-circuit detection and shutdown are operational and WS2410AT is protected but the $V_{CSO(TH)}$ parameter, hence the short-circuit detection depends on V_S and V_{EN}. A dedicated function named DESAT covers the protection threshold in the $V_{S(SC)LOW}$ range.

The variation of $V_{CSO(TH)}$ is shown in the following graphs.

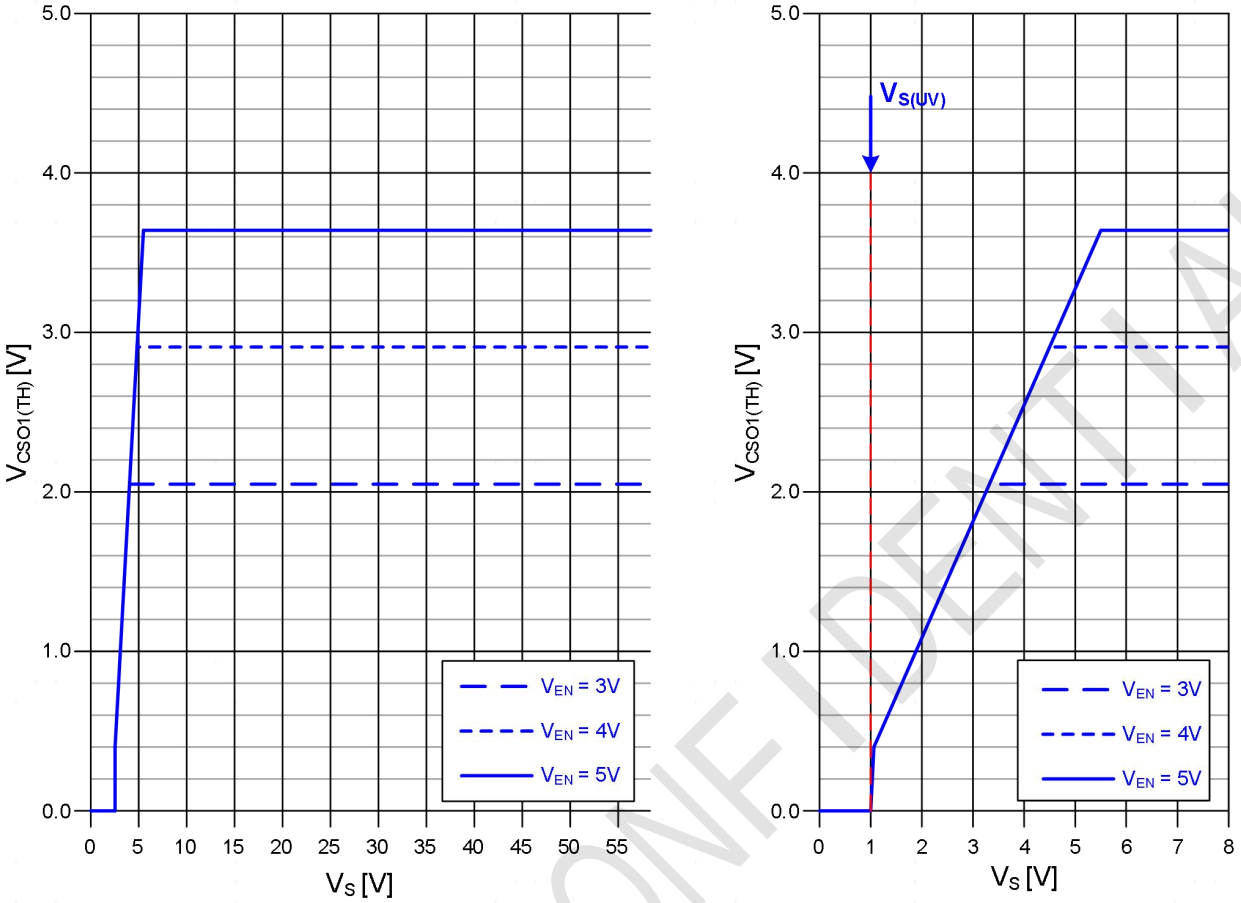


Figure 14. Typical $V_{CSO1(TH)}$ versus V_S and V_{EN} (independent of T_J)

Undervoltage protection on VS

VS pin has an integrated comparator comparing permanently VS voltage to $V_{S(UV)}$ reference, which allows WS2410AT to enter SAFESTATE mode when VS reaches down $V_{S(UV)}$ level.

The turn-off delay time is computed by the sum $t_{DUV(H)INT(L)}$ + $t_{DINT(L)G(L)}$.

This has two consequences:

- The driver is protected down to 0 V on battery, meaning that a very strong short-circuit that would actually bring the voltage on VS node to 0 V is covered and switch is protected.
- The driver could be sensitive to micro-cuts on the supply if the micro-interruptions are longer than $t_{DUV(H)INT(L)}$.

To overcome this effect, a capacitor can be used next to VS pin (e.g. a few micro-farad). Additionally, if large micro-cuts are expected in the application, EN pin can be connected to VS pin directly through a 100kΩ (or more) resistor. An additional Zener diode is necessary on the ENABLE pin to limit the voltage to the desired value, e.g. 3.3 V or 5 V. When the micro-interruption is over, the driver will automatically turn-on again as soon as $V_{EN(H)}$ (PRQ-74) threshold is reached again on the EN pin.

See "Operating modes" for details on diagnostics in SAFESTATE mode.

Once in SAFESTATE mode, the driver needs to be reset.

The figure below shows the diagram, (1), the normal driver configuration, and (2), a possible adapted configuration with external circuitry for connection of the ENABLE pin to VS which will reset the driver automatically in case of a large micro-interruption.

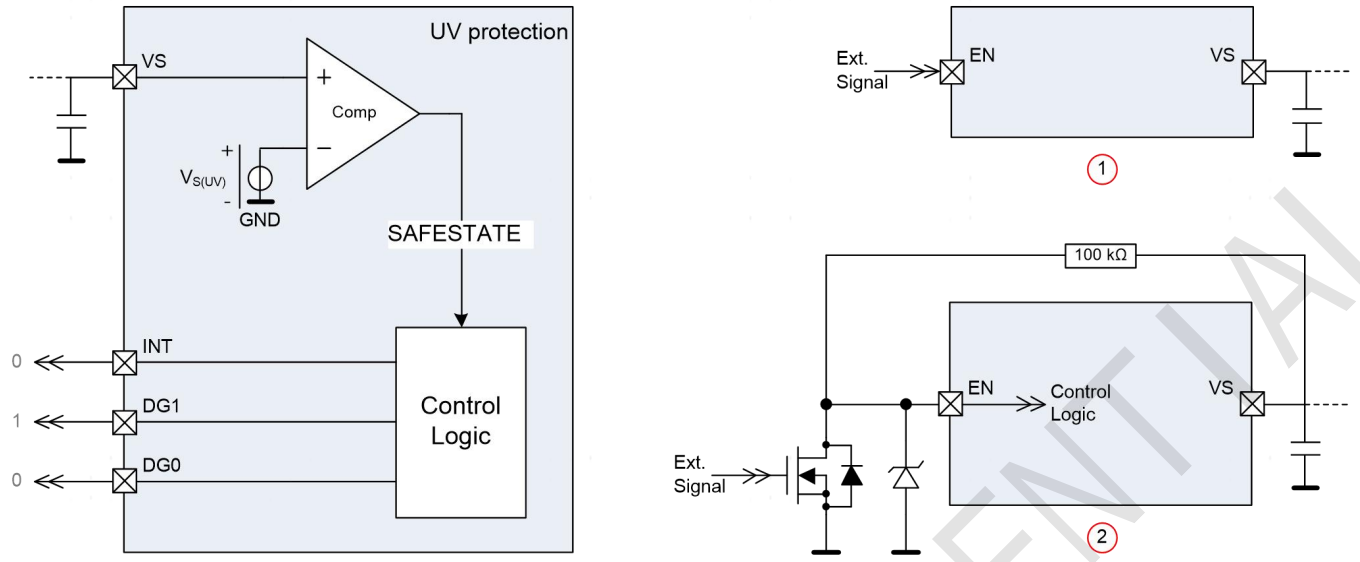


Figure 15. $V_{S(UV)}$ protection diagram and possible driver configuration

Custom protections with comparator

WS2410AT features a voltage comparator with inputs CPP and CPN.

This comparator can be used to trigger SAFESTATE mode based on any analog voltage, even a voltage external to WS2410AT.

CPP is the positive input of the comparator and CPN is the negative input.

VCPREF can be adjusted by microcontroller, or fixed by an on-board power supply chip, such as an Infineon SBC, or a simple voltage divider, within the limits $V_{CP(REF)}$ for stability.

Using this comparator allows WS2410AT to enter SAFESTATE and turn-off MOSFET independently from the microcontroller. The comparator reacts with a delay time $t_{DCP(H)INT(L)}$. Consequently the turn-off delay time in case of shutdown by comparator CP can be computed by the sum $t_{DCP(H)INT(L)} + t_{DINT(L)G(L)}$.

When SAFESTATE mode is triggered, digital outputs {DG0;DG1} will feedback {1;1}. See "Operating modes". Once in SAFESTATE, driver needs to be reset.

Below are illustrated 4 possible use cases, and more are possible:

Case 1: overtemperature protection using TMPO output.

Case 2: I-t wire protection using RC. Both limits, short-reaction time and long-time direct current are adjustable dynamically (e.g. a microcontroller PWM output) with VEN and VCPREF respectively.

Case 3: protection using any external signal. The VCP(REF) can be dynamically adjusted by microcontroller. For example, for battery switch application, the current feedback from BMS can be used to trigger the SAFESTATE mode.

Case 4: undervoltage protection by monitoring VS with simple voltage divider.

Note: this custom protection is available together with the short-circuit comparator on CSA1 output.

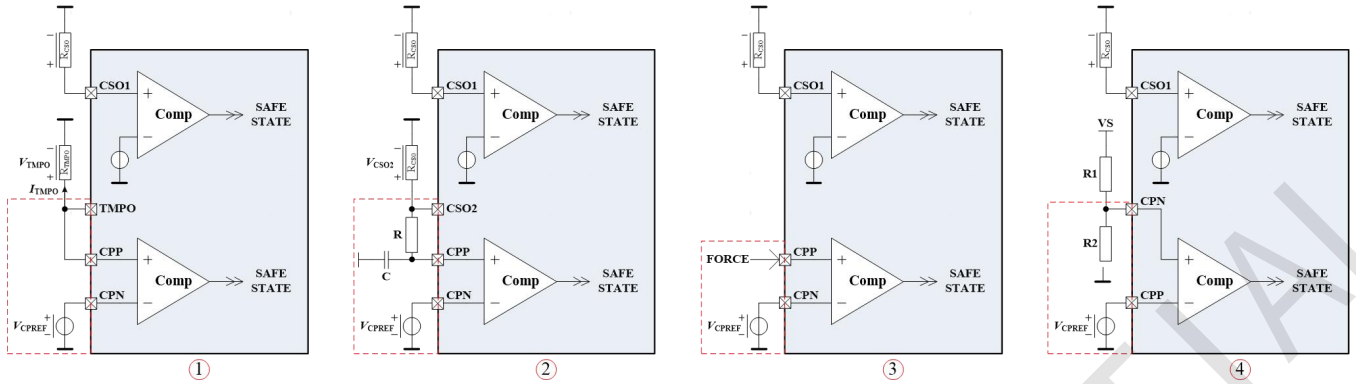


Figure 16. Comparator use cases examples

Gate undervoltage lock-out protection

The purpose of the gate undervoltage lock-out protection **UVLO** is to avoid to drive MOSFET in linear mode due to a leakage on boost converter output or MOSFET gates.

If V_{BC} - V_S < UVLO in ON mode, the driver enters SAFESTATE mode.

UVLO protection function is activated in ON mode, if at least V_{BC} - V_S has satisfied the condition V_{BC} - V_S > $V_{BC(TH)}$ at least once in ON mode.

If V_{BC} - V_S < UVLO in ON mode and $V_{BC(TH)}$ has not been reached once in ON mode, the device does not enter SAFESTATE mode because UVLO is not activated, but **gates do not turn on**.

As a result this situation can be detected by INT = 1 and DG0 displaying the maximum frequency of the boost converter, given the implemented boost converter external components. Once in SAFESTATE, driver needs to be reset.

Reset of SAFESTATE

WS2410AT has one way to actively reset the SAFESTATE: the voltage on EN pin needs to be pulled low for t_{RESET}.

Set V_{EN} < $V_{EN(L)}$ for t_{RESET}. See Figure 2 for timing diagram.

Once EN pin is pulled down, INT signal will go up one the driver reaches SLEEP state again.

SLEEP state can be verified by DG0 = DG1 = low.

WS2410AT can move back to IDLE mode by EN=high and INA=INB=low.

Note: If INA or INB remain "high" when EN is set "high", the driver will immediately enter ON mode if the condition V_{BC} - V_S ≥ $V_{BC(TH)}$ is satified.

Driver supply: boost converter

A boost DC/DC converter structure is the supply of WS2410AT.

The diode and the activation switch K1 are implemented in the driver, but the capacitor C_{BC}, the resistor R_{RS} and the inductor L1 have to be added as external components.

The boost converter is active in IDLE mode, ON mode, SAFESTATE mode. It is off in SLEEP mode.

The boost converter starts when V_S ≥ $V_{S(NOR)}$ and V_{EN} ≥ $V_{EN(H)}$. Then, once V_{BC} - V_S ≥ $V_{BC(TH)}$, the boost converter operates normally over the $V_{S(EXT)}$ range. If V_{EN} ≤ $V_{EN(L)}$, the driver goes back to SLEEP mode from any of the other three operating modes and the boost converter is stopped.

The switch K1 activation time is reflected on pin DG0 in ON mode.

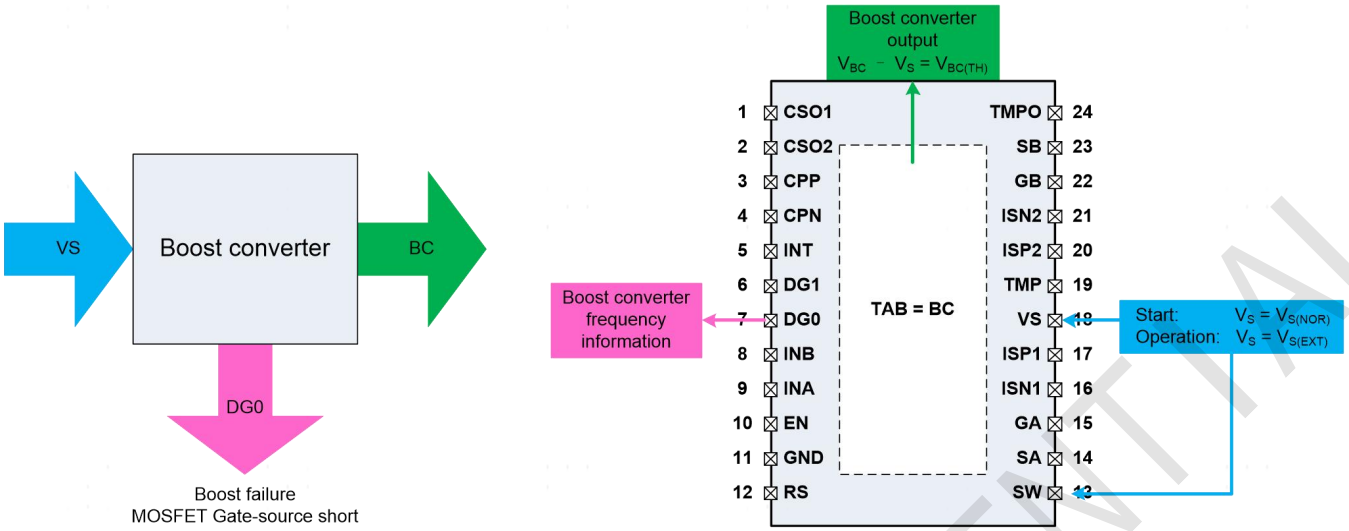


Figure 17. Principle of boost converter as driver supply

The topology of the WS2410AT supply is a boost DC/DC converter working in current mode control.

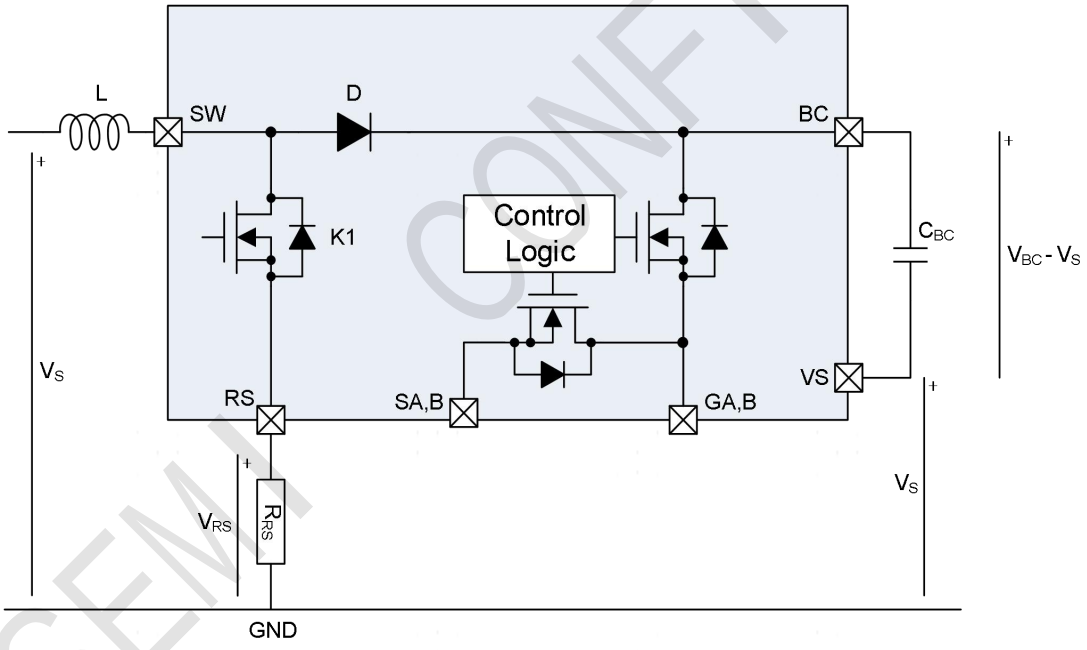


Figure 18. BC topology used as gate supply

Activation:

K1 is an integrated MOSFET, switched on when V_{BC} - V_S < $V_{BC(TH)}$ and V_{RS} < $V_{RS(TH)}$.

K1 is turned off when V_{RS} > $V_{RS(TH)}$ or V_{BC} - V_S > $V_{BC(TH)}$.

The inductor charges the C_{BC} capacitor through diode D.

D has a forward voltage drop of V_{FBC}.

The K1 MOSFET cannot restart during $t_{BC(OFF)}$ after $V_{RS(TH)}$ has been reached. This limits the boost converter maximum frequency.

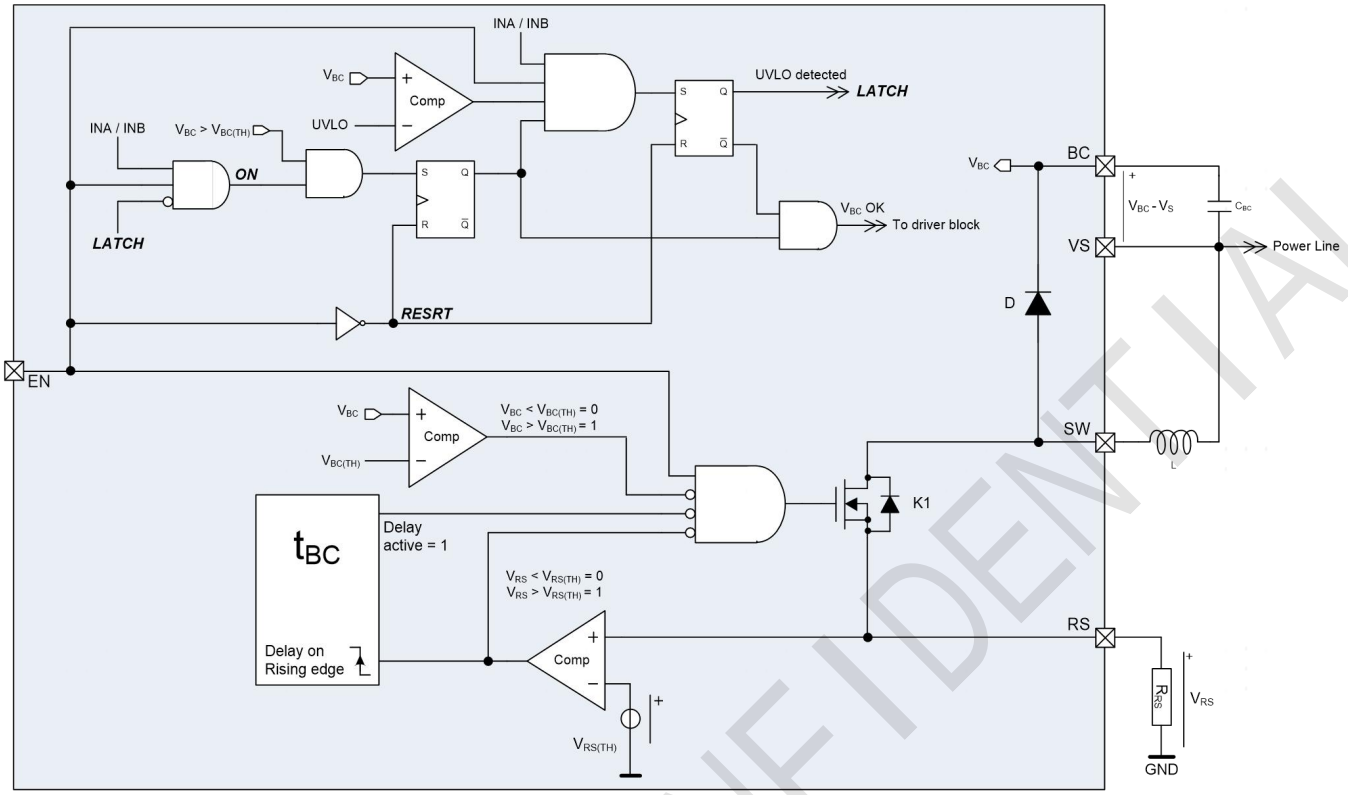


Figure 19. Boost converter control logic

The current in the inductor is limited by the $V_{RS(TH)}$ comparator which monitors the voltage across RRS. Due to the delay in the loop, $t_{D(OFF)K1}$, the inductor current exceeds the threshold set by: $V_{RS(TH)}$.

The current waveform in the inductor is not linear, but exponential, because the sum of the resistance of K1, of the parasitic inductor of L1 (R_L), and R_{RS} are not negligible in the K1 short activation timeframe.

The calculations are described in the application note "Getting started with WS2410AT".

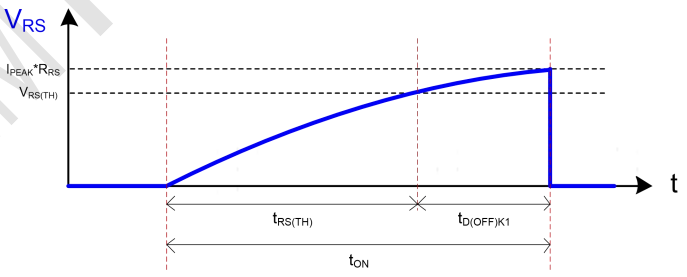


Figure 20. Current peak control

The peak current must not exceed the maximum rating of I_{SW}.

MOSFET connections in application

The next figure shows a few typical connections in which the WS2410AT driver can operate.

Amplifiers CSO1 and/or CSO2 can be disconnected to reduce WS2410AT self-consumption. See “Current senses in ON and SAFESTATE modes Figure 11”.

Any custom protection signal can be connected to the additional comparator regardless of the power MOSFET structure used, see "Custom protections with comparator".

See "Table 1" on what to do with non-used pins.

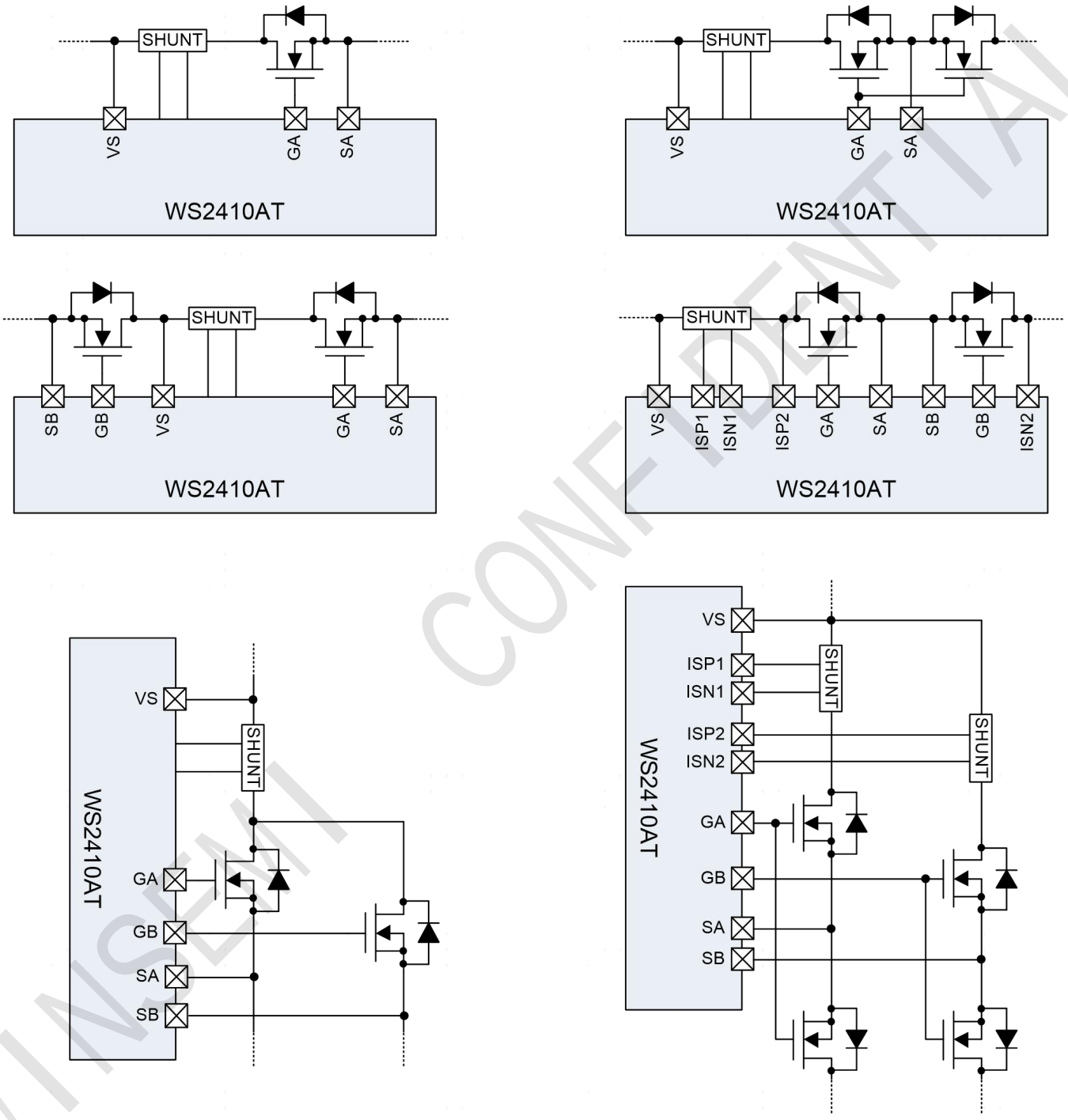
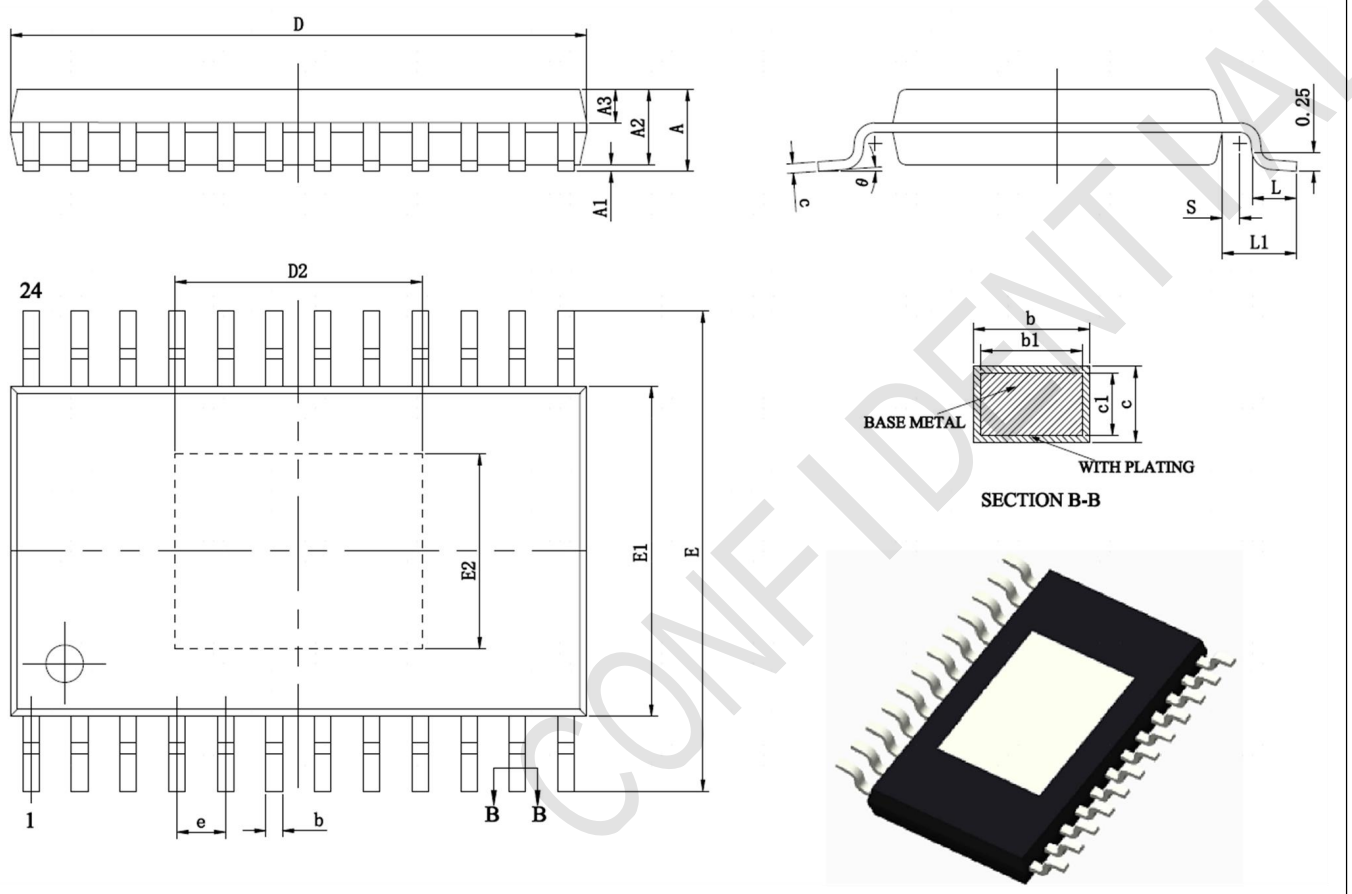


Figure 21. Typical MOSFET and shunt resistor connections

Package Outline

eTSSOP24L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.2
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
C1	0.12	0.13	0.14
D	7.70	7.80	7.90
D2	4.73	-	4.93
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.75	-	2.95
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

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