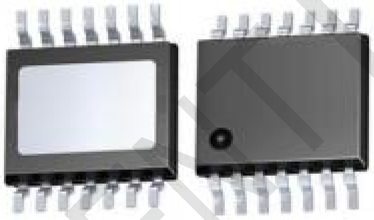
WS9008AE
Smart High-Side Power Switch Single Channel，ESSOP14 ，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V automotive applications

Package	ESSOP14
Marking	WS9008AE
	

Basic Features

- Single channel device
- Very low stand-by current
- 3.3V and 5 V compatible logic inputs
- Switch ON capability while Inverse Current condition (Inverse ON)

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage($T_j \geqslant 25$ °C)	V_S	35V
Operating voltage range	V_{NOM}	4.1-28V
On-state resistance (per channel)(T_j=150 °C)	R_{ON}	22mΩ
Nominal load current (one channel active)(T_A=85°C)	$I_{L(NOM)}$	10A
Typical current sense ratio	K	6500
Current limitation	I_{LIMH}	80A
Supply current in sleep	I_{SLEEP}	0.6uA

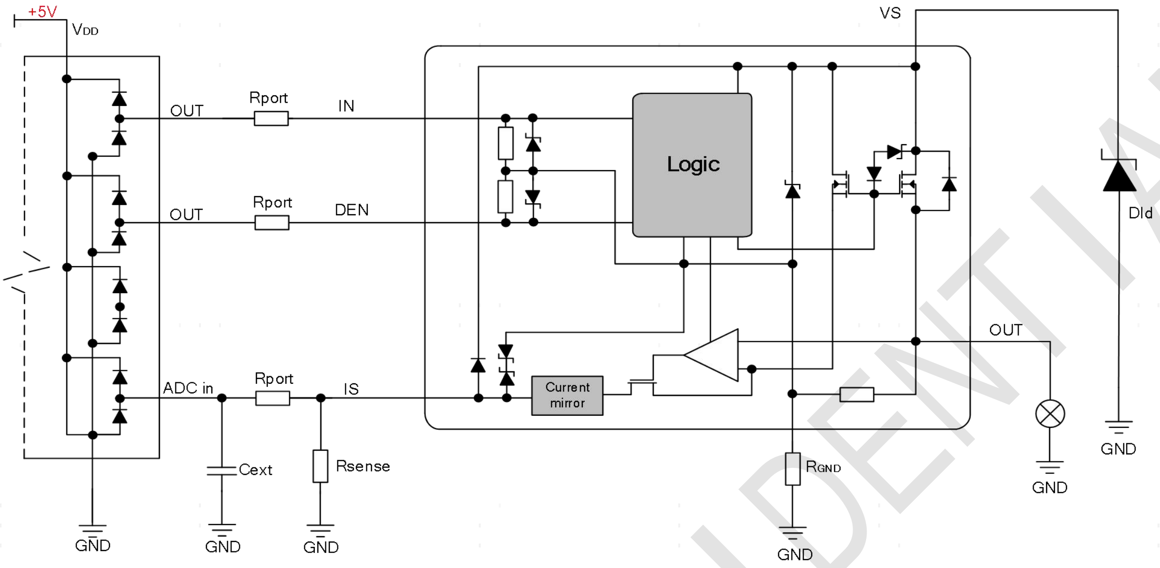
Diagnostic Functions

- Proportional load current sense
- High current sense precision for wide range currents
- Off-state open load detection
- Output short to VS detection
- Overload and short to ground latch-off
- Thermal shutdown latch-off
- Very low current sense leakage

Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VS
- Thermal shutdown
- Electrostatic discharge protection

Typical Application Circuit

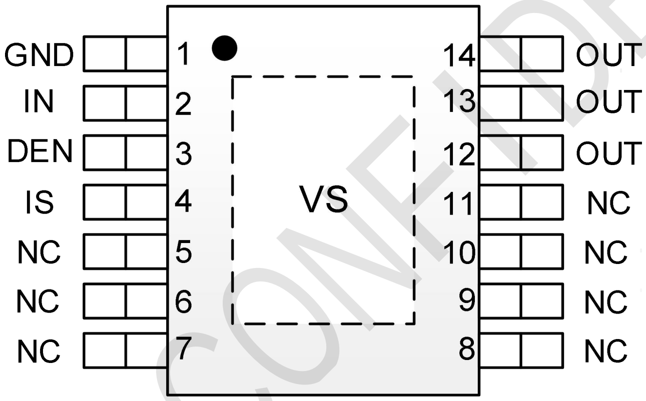


Ordering Information

Package	Top Mark	Part No.
ESSOP14L, Pb-free	WS9008AE XXYMXX	WS9008AE

Pin Configuration

Top view



Pin Description

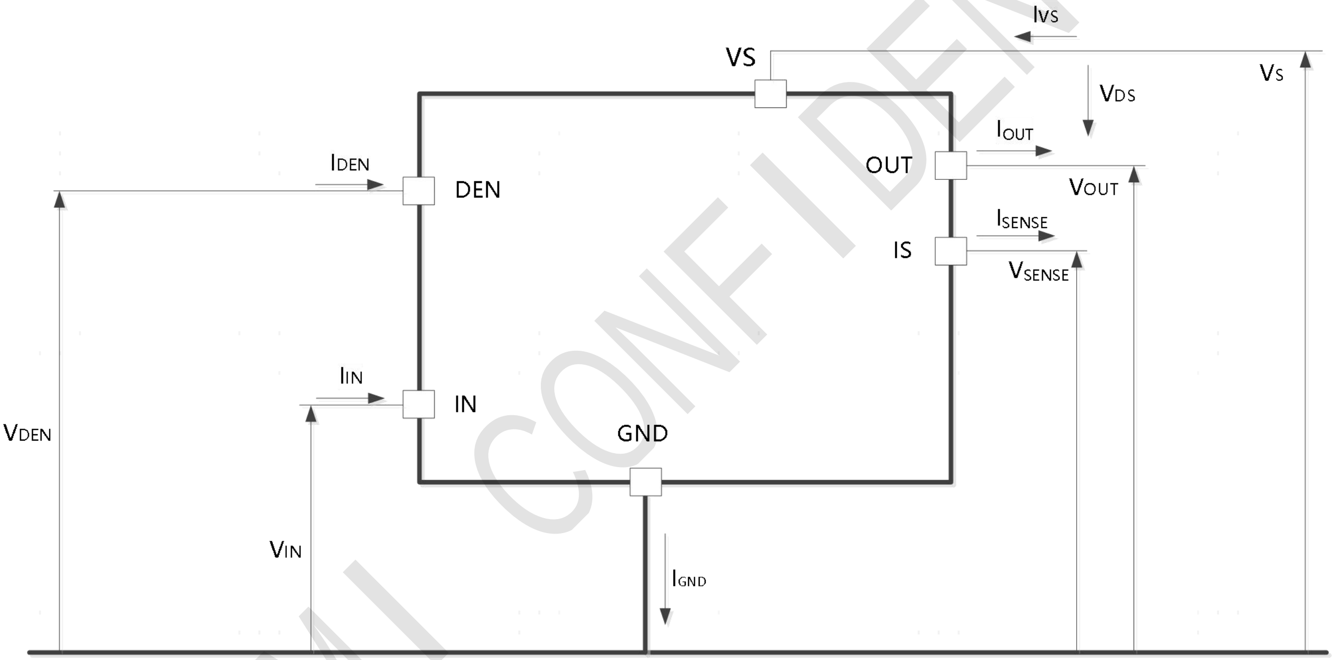
Pin Name	Pin NO.	Pin Description
GND	1	Ground connection. Must be reverse battery protected by an external diode / resistor network.
IN	2	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
DEN	3	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the IS diagnostic pin.
IS	4	Multiplexed analog sense output pin; it delivers a current proportional to the load current.
NC	5/6/7/8/9/10/11	Not Connected
OUT	12/13/14	Power outputs.
VS	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	IS	OUT	IN	DEN
Floating	Not allowed	X(1)	X	X
To ground	Through 1K resistor	Not allowed	Through 15K resistor	Through 15K resistor

Note1：X do not care.

Current and Voltage Conventions



Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_S	DC supply voltage(T_j≥25 °C)	35	V
$-V_S$	Reverse DC supply voltage（T≤2min，T_A=+25℃）	16	V
Vsc(vs)	Max Supply Voltage for Short Circuit Protection	24	V
I_{GND}	ground pin current	-50 to 50	mA
I_{OUT}	OUT DC output current	Internally limited	A
I_{IN}, I_{DEN}	Current through V_{IN}, V_{DEN} Pin	-1 to 3	mA
I_{SENSE}	IS pin DC output current	I_{SENSEH_MAX}	mA
	IS pin DC output current in reverse	-20	
V_{IS}	Voltage at IS Pin	-8 to 6	V
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

ESD Susceptibility (Note4)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}{}^{3)}$	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	±4	kV
$V_{ESD(CDM)}{}^{4)}$	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	±750	V

Note4：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

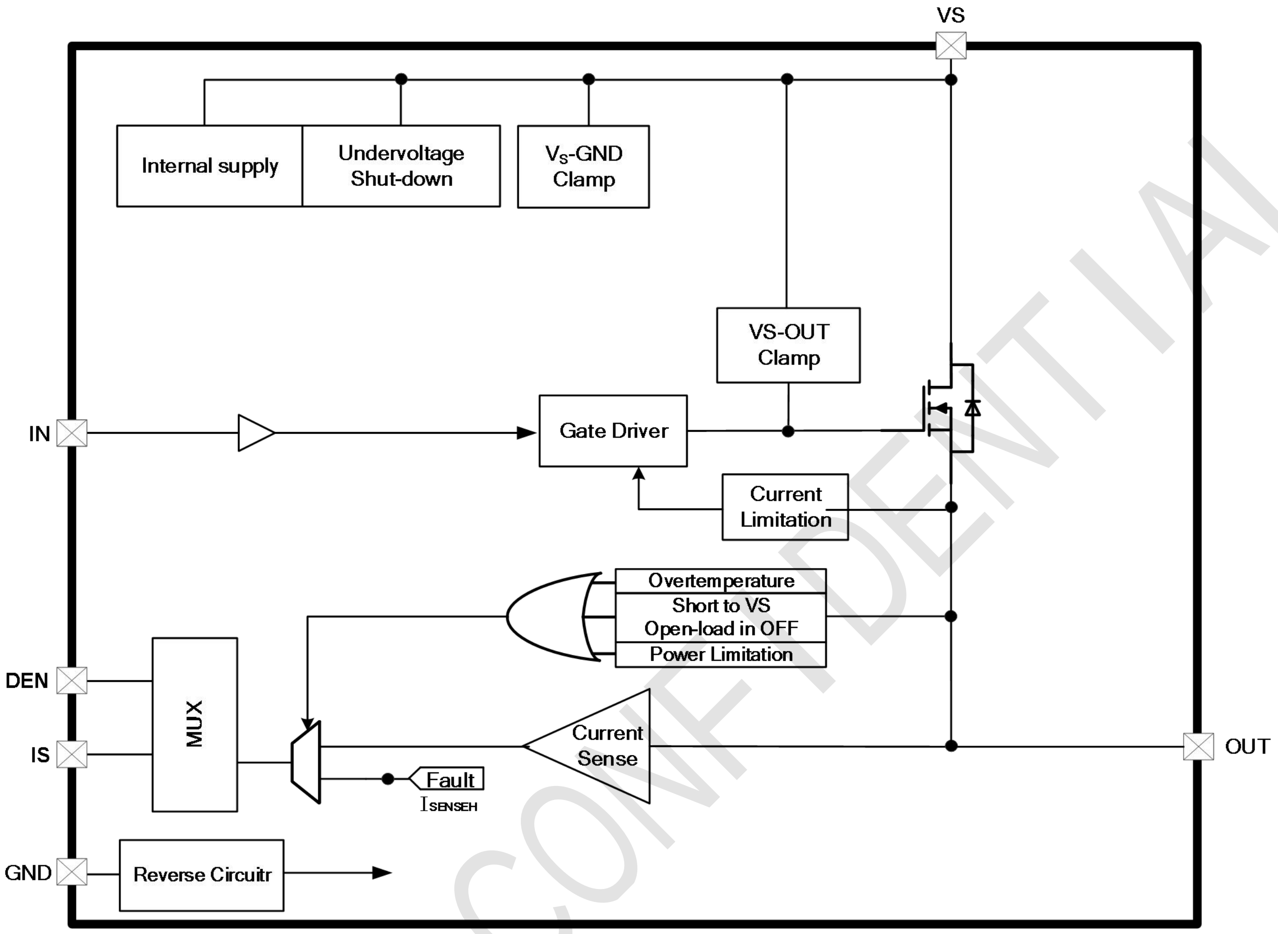
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

Thermal Resistance (Note5)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	28	℃/W

Note5：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Functional Block



Electrical Characteristics (Note6) , 6V <VS < 18 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		4.1	13	28	V
Under voltage shutdown	V_{USD}				4.0	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=3A, T_j = 25℃		10		mΩ
		I_{OUT}=3A, T_j =150℃			22	
		I_{OUT}=3A, V_S =4.5V, T_j = 150℃			25	
Nominal load current	$I_{L(NOM)1}$	T_A=25℃		12		A
Nominal load current at T_A=85℃	$I_{L(NOM)1\_85}$	T_A=85℃, T_j < 150℃		10		A
Inverse Current Capability	$I_{L(INV)}$	V_S<V_{OUT}, V_{IN}=5V, T_A=25℃		10		A
V_S clamp voltage	V_{CLAMP}	I_{VS}=5 mA	33	38	44	V
Supply current in sleep	I_{SLEEP}	V_S=13V, V_{IN}=V_{OUT}=V_{DEN} =0V T_j =25℃		0.6	3.0	μA
		V_S =13V, V_{IN}=V_{OUT}=V_{DEN} =0V, T_j= 125℃			6.0	μA
Sleepy mode blanking time	t_{D_SLEEP}	V_S=13V, V_{IN}=V_{OUT}=0V V_{DEN}=5V to 0V	150	350	700	us
Supply current in active	$I_{S(ACTIVE)}$	V_S=13V, V_{DEN}=5V, V_{IN}=0V,		0.8	1.6	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_S=13,V_{DEN}=5V, V_{IN}=5V		1.5	3.0	mA
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_S=13V, T_j =25℃	0	0.1	3	μA
		V_{IN} =V_{OUT}=0V, V_S=13V, T_j =125℃	0		6	μA
Output - V_S diode voltage	V_F	I_{OUT} =-1A, T_j =150℃			0.7	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	VS=13V,V_{DEN}=5V,R_L=3Ω		10	40	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$			20	80	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	VS=13V,V_{DEN}=5V,R_L=3Ω	0.1	0.5	1.0	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		0.1	0.6	1.2	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	VS=13V,V_{DEN}=5V,R_L=3Ω	-50		50	us

Logic input (IN, DEN)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_L				0.9	V
Low level logic input current	I_L	V_{INL}=0.9V	2	16	32	uA
Logic input high level voltage	V_H		2.1		6.0	V
High level logic input current	I_H	V_{INH} =2.0V	4	20	40	uA
Logic input hysteresis voltage	$V_{(hyst)}$		-	0.25	-	V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	6V < V_S< 18V ,V_{DS}=10V	65	80	100	A
		V_{DS} > 22V		48		
Short circuit current during thermal cycling	I_{LIML}	V_S=13V, V_{DEN}=5V, T_R<T_j<T_{TSD},		20		
Counter Reset Delay Time after Fault Condition	T_{reset}	V_S=13V		70		ms
Maximum number of Short mode latch				5	-	cycles
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		80		℃
Current limit thermal hysteresis	T_R			40		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=2A, L= 3mH, T_j =-40℃ to 150℃	V_S-33	V_S-38	V_S-44	V

Current sense characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
I_{OUT}/I_{SENSE}	K_0	I_{OUT}=0.1A,V_{DEN}=5V	-10%	6080	+10%	
I_{OUT}/I_{SENSE}	K_1	I_{OUT}=0.5A, V_{DEN}=5V	-6%	6500	+6%	
I_{OUT}/I_{SENSE}	K_2	I_{OUT}=1A, V_{DEN}=5V	-3%	6500	+3%	
I_{OUT}/I_{SENSE}	K_3	I_{OUT}=3A, V_{DEN}=5V	-3%	6500	+3%	
I_{OUT}/I_{SENSE}	K_4	I_{OUT}=6A, V_{DEN}=5V	-3%	6500	+3%	
Current sense leakage current	I_{SENSE0}	IS disabled: V_{DEN} =0V	0		1	uA
		IS enabled:V_{DEN} = 5V, channel ON, I_{OUT}= 0A	0		3	
Output voltage for IS shutdown	V_{OUT_MSD}	V_{DEN}=5V, R_{SENSE}=3.9K, V_{IN}=5V;		5		V
Max analog sense output voltage	V_{SENSE}	V_S=13V, V_{SENSE} =5V	4.5			V
Current sense output current in fault condition	I_{SENSEH}	V_S=13V, V_{SENSE} =5V	5	10	15	mA
Current sense output voltage in fault condition	V_{SENSEH}	V_S=13V, V_{SENSE} =5V	5.5	6.6	7.0	V

OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold（VS-OUT）	V_{OL}	V_{DEN} =5V, V_{IN}=0V	2.5	3.5	4.5	V
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{DEN}=5V, V_{IN}= 5V to 0V,V_{OUT} =V_S,	150	350	700	us
Settling time for valid OFF-state open load diagnostic indication from rising edge of DEN	$t_{D\_OL\_V}$	V_{IN}=0V,V_{OUT}=V_S,V_{DEN}=0V to 5V			150	us

OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	V_{DEN}=5V,V_{IN}=0V, V_{OUT}=V_S-4.5V to V_S		5	30	us

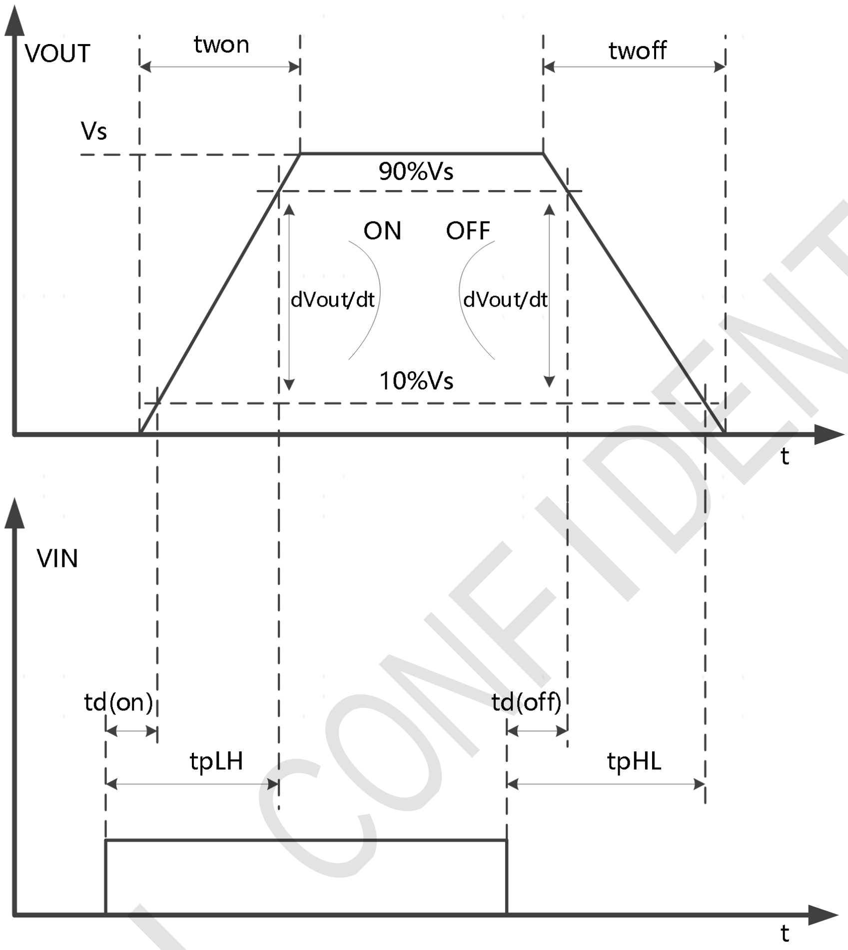
Current sense timings

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense settling time from rising edge of DEN	$t_{DSENSE1H}$	V_{IN}=5V, V_{DEN}=0V to 5V, R_{SENSE}=1.2K, R_L=3Ω			100	us
Current sense disable delay time from falling edge of DEN	$t_{DSENSE1L}$	V_{IN}=5V, V_{DEN}=5V to 0V, R_{SENSE}=1.2K, R_L=3Ω		5	20	us
Current sense settling time from rising edge of IN	$t_{DSENSE2H}$	V_{IN}=0V to 5V, V_{DEN}=5 V, R_{SENSE}=1.2K, R_L=3Ω		80	250	us
Current sense settling time from rising edge of I_{OUT}(dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$	V_{IN}=5V, V_{DEN}=5V, R_{SENSE}=1.2K, I_{SENSE}=90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} R_L=3Ω			150	us
Current sense turn-off delay time from falling edge of IN	$t_{DSENSE2L}$	V_{IN}=5V to 0V, V_{DEN}=5V, R_{SENSE}=1.2K, R_L=3Ω		80	250	us

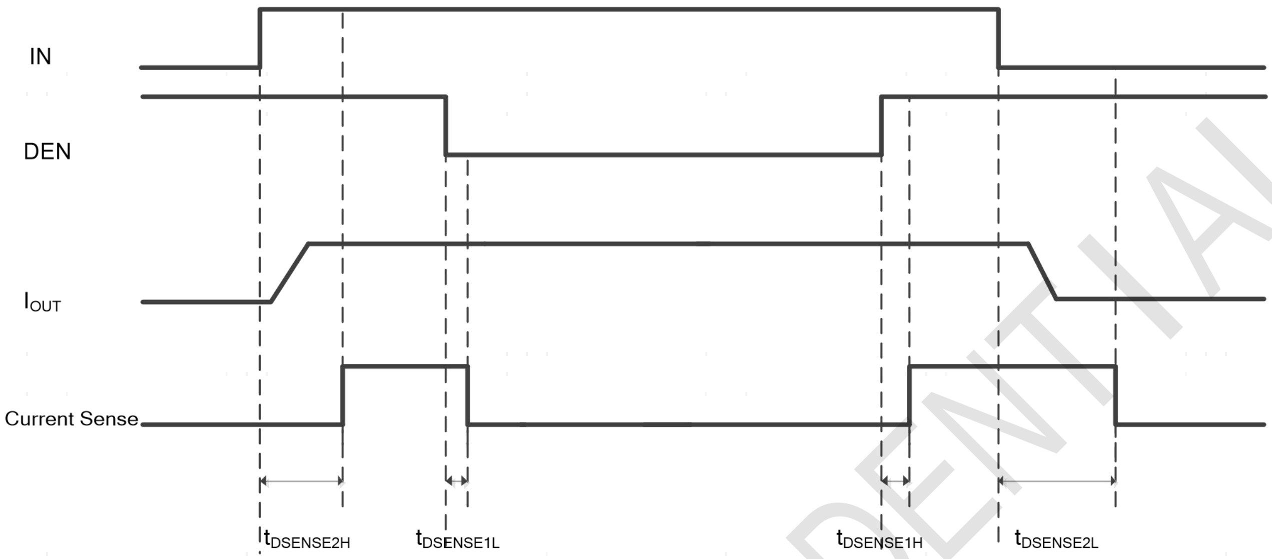
Note6: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

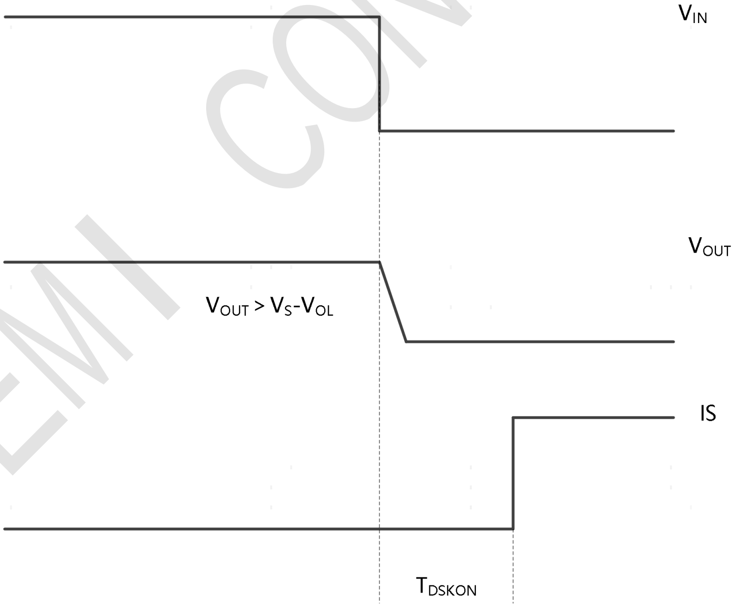


Table 2. Truth table

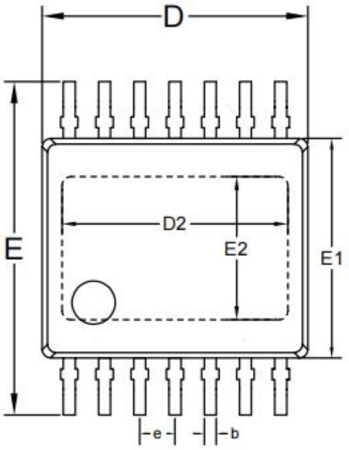
Conditions	IN	DEN	OUT	Current sense
SLEEP	L	L	L	0
Normal	L	H	L	0
	H	H	H	$I_{SENSE} = I_{OUT}/K$
Overload	H	H	L	I_{SENSEH}
Over Temperature	L	H	L	0
	H	H	Z	I_{SENSEH}
Undervoltage	X	X	L	0
Short to V_S	L	H	H	I_{SENSEH}
	H	H	H	<Normal
Open-Load	L	H	H	I_{SENSEH}
Short circuit to GND	H	H	L	I_{SENSEH}

Table 3. Current sense output

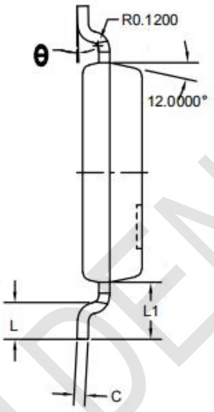
DEN	MUX Channel	Current sense output			
		Normal	Overload	OFF-state	Negative output
L		Hi-Z			
H	Channel diagnostic	$I_{SENSE} = I_{OUT}/K$	$I_{SENSE} = I_{SENSEH}$	$I_{SENSE} = I_{SENSEH}$	Hi-Z

Package Outline

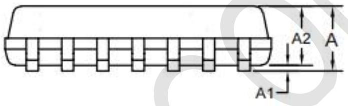
ESSOP14



TOP VIEW



SIDE VIEW



SIDE VIEW

SYMBOLS	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.200
A1	0.000	0.050	0.100
A2	1.050	1.100	1.150
b	0.200	0.250	0.300
C	0.203BSC		
D	4.850	4.900	4.950
D2	3.900	4.000	4.100
E	6.100	6.150	6.200
E1	4.000	4.050	4.100
E2	2.550	2.650	2.750
e	0.65BSC		
L	0.625	0.675	0.725
L1	1.05BSC		
θ	0°	3°	6°

CONTACT

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