

WST6010AN**Smart High-Side Power Switch Single Channel, 9mΩ, DFN9×6-14L , AEC-Q100 qualified****Application**

- ◆ Suitable for resistive, inductive and capacitive loads
- ◆ Replaces electromechanical relays, fuses and discrete circuits
- ◆ Most suitable for loads with high inrush current, such as lamps
- ◆ Suitable for 12 V and 24 V trucks + trailer and transportation systems

Basic Features

- ◆ Single channel device
- ◆ Very low stand-by current
- ◆ 3.3 V and 5 V compatible logic inputs
- ◆ Optimized electromagnetic compatibility
- ◆ Very low electromagnetic susceptibility

Diagnostic Functions

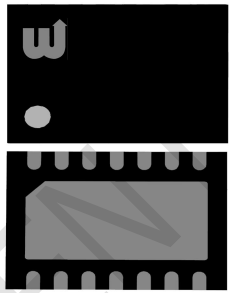
- ◆ Proportional load current sense
- ◆ High current sense precision for wide range currents
- ◆ Off-state open load detection
- ◆ OUT short to VS detection
- ◆ Overload and short to ground latch-off
- ◆ Thermal shutdown latch-off
- ◆ Very low current sense leakage

Protection Functions

- ◆ Undervoltage shutdown
- ◆ Overvoltage clamp
- ◆ Load current limitation
- ◆ Self limiting of fast thermal transients
- ◆ Protection against loss of ground and loss of VS
- ◆ Thermal shutdown
- ◆ Electrostatic discharge protection

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_S	60V
Operating voltage range	V_{NOM}	8-36V
On-state resistance ($T_J = 25^\circ\text{C}$)	R_{ON}	9mΩ
Nominal load current ($T_J = 25^\circ\text{C}$)	$I_{L(NOM)}$	13A
Typical current sense ratio ($I_{OUT}=4A$)	K	5250
Current limitation	I_{LIMH}	75A
Supply current in sleep	I_{SLEEP}	3uA

Package	DFN9×6-14L
Marking	WST6010AN
	

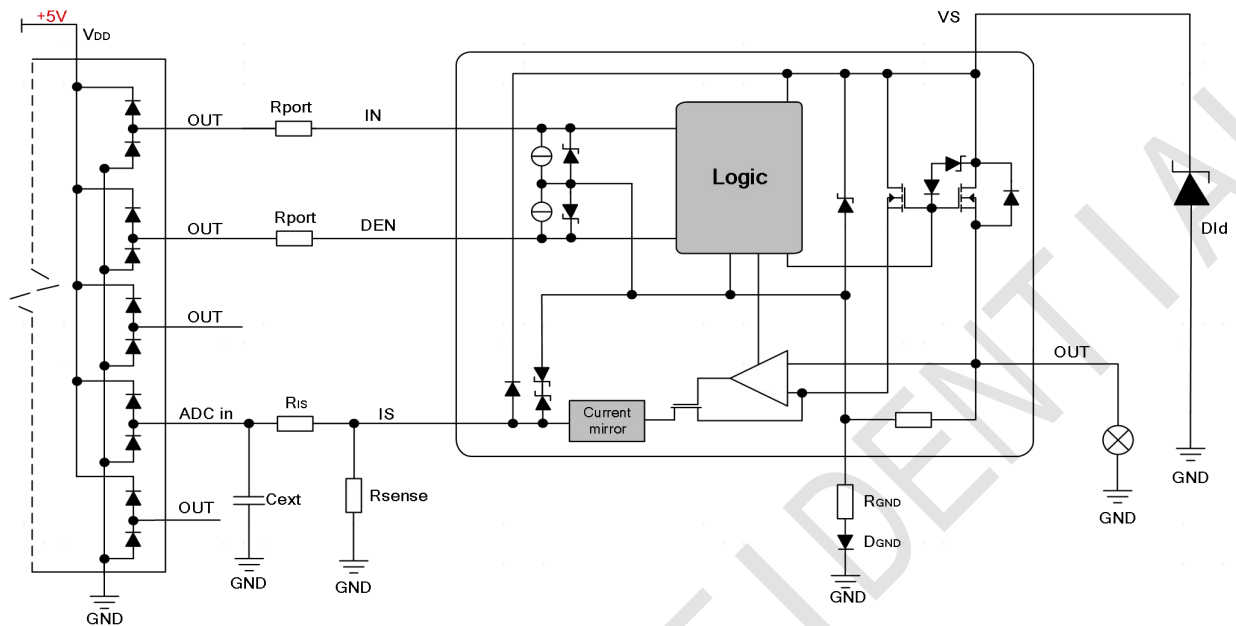


RoHS

ISO 26262
ready

Halogen-free

Typical Application Circuit



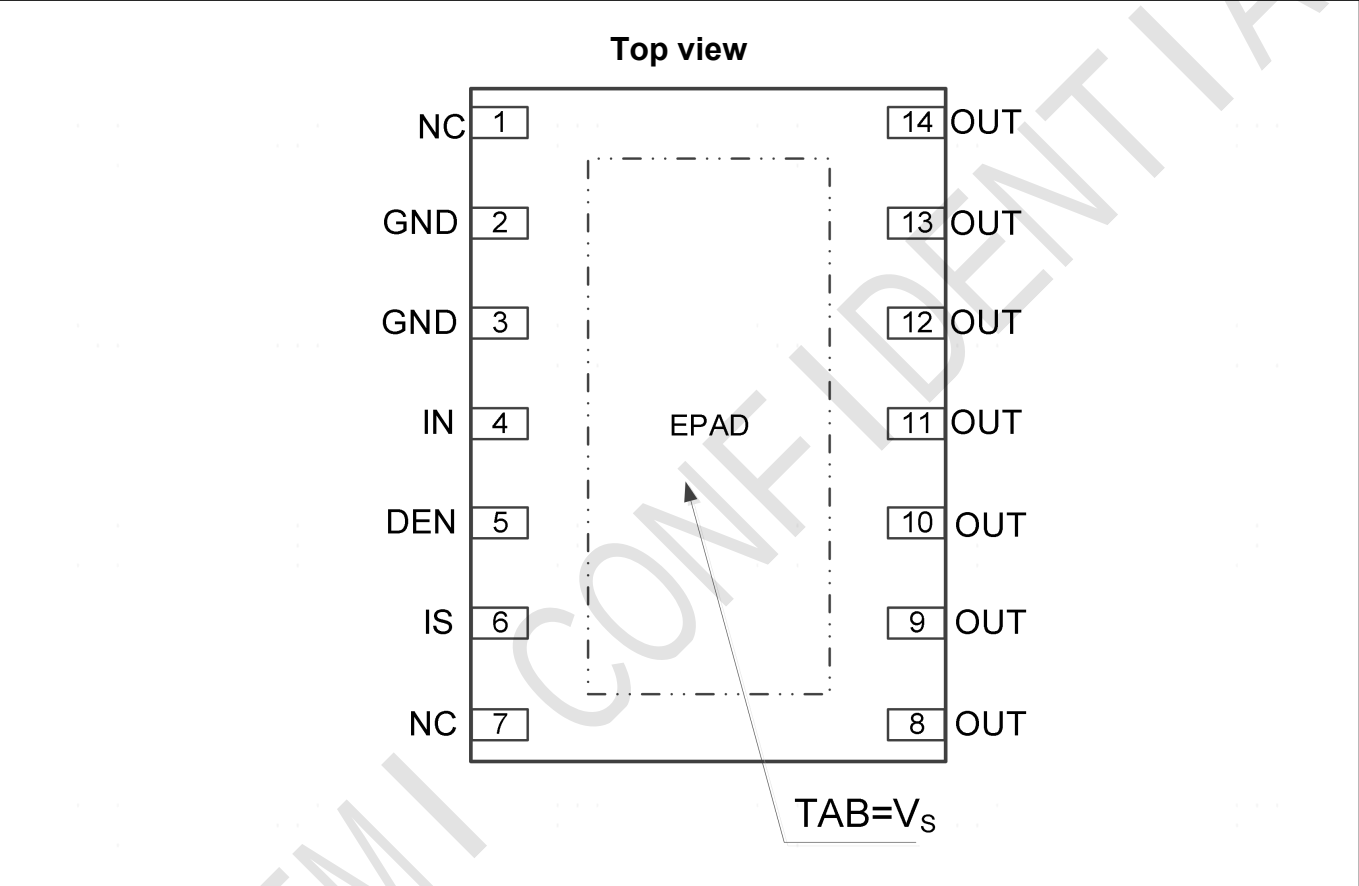
Note1:

- 1) For D_{GND} , the diode with lower V_F is advisable.
- 2) For R_{IS} and C_{EXT} , 100k Ω resistor and 10nF capacitor are advisable..

Ordering Information

Package	Top Mark	Part No.
DFN9×6-14L, Pb-free	WST6010AN XXYMX	WST6010AN

Pin Configuration



Pin Description

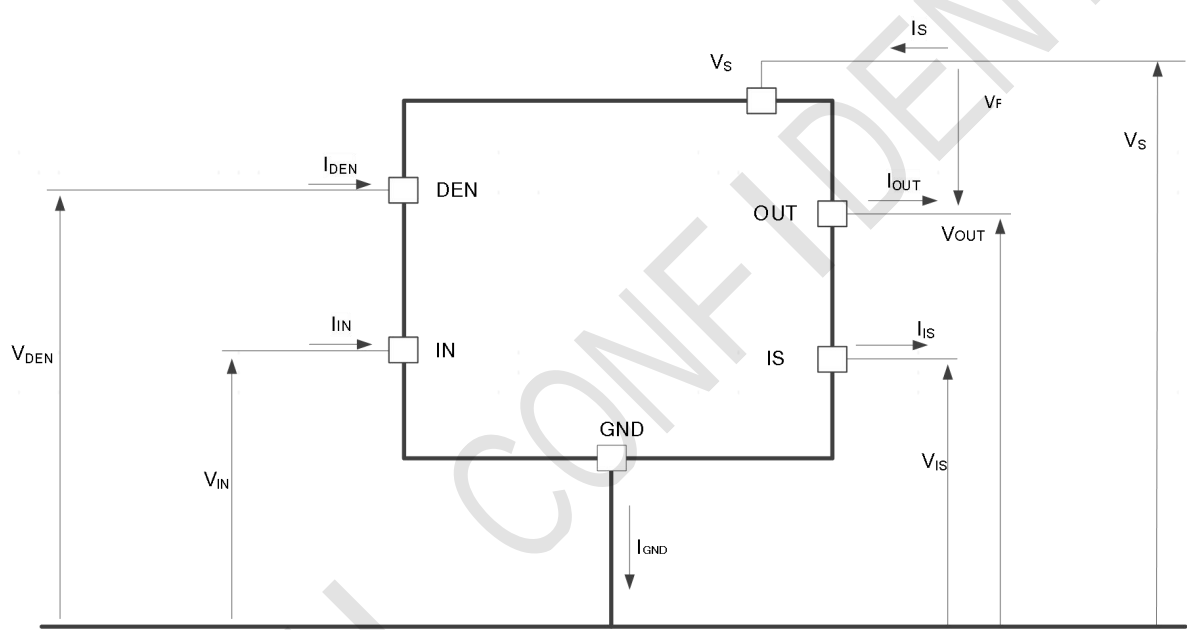
Pin Name	Pin NO.	Pin Description
NC	1	Not Connected
GND	2/3	Ground connection. Must be reverse battery protected by an external diode / resistor network.
IN	4	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
DEN	5	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the IS diagnostic pin.
IS	6	Multiplexed analog sense output pin; it delivers a current proportional to the load current.
CL	7	Adjustable current limit. floating if external current limit is not need.
OUT	8/9/10/11/12/13/14	Power outputs.
VS	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	IS	OUT	IN	DEN
Floating	Not allowed	X ⁽¹⁾	X	X
To ground	Through 1.0K resistor	Not allowed	Through 15K resistor	Through 15K resistor

Note2: X do not care.

Current and Voltage Conventions



Note3: $V_F = V_{OUT} - V_S$ during reverse battery condition.

Absolute Maximum Ratings (Note4)

Symbol	Parameter	Value	Unit
V_s	Transient supply voltage	60	V
$-V_s$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUT DC output current	Internally limited	A
V_{IN}, V_{DEN}	IN, DEN DC input voltage	-0.3 to 6.0	V
I_{IS}	IS pin DC output current	20	mA
	IS pin DC output current in reverse	-20	
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

Note4: Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note5)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	°C/W
T_{JA}	Junction-to-Ambient Thermal Resistance	30	°C/W

Note5: According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note6)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}^{(3)}$	ESD Susceptibility all Pins (HBM)	± 2	kV
$V_{ESD(HBM)_{OUT}}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	± 4	kV
$V_{ESD(CDM)}^{(4)}$	ESD Susceptibility all Pins (CDM)	± 500	V
$V_{ESD(CDM)_{CORN}}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	± 750	V

Note6:

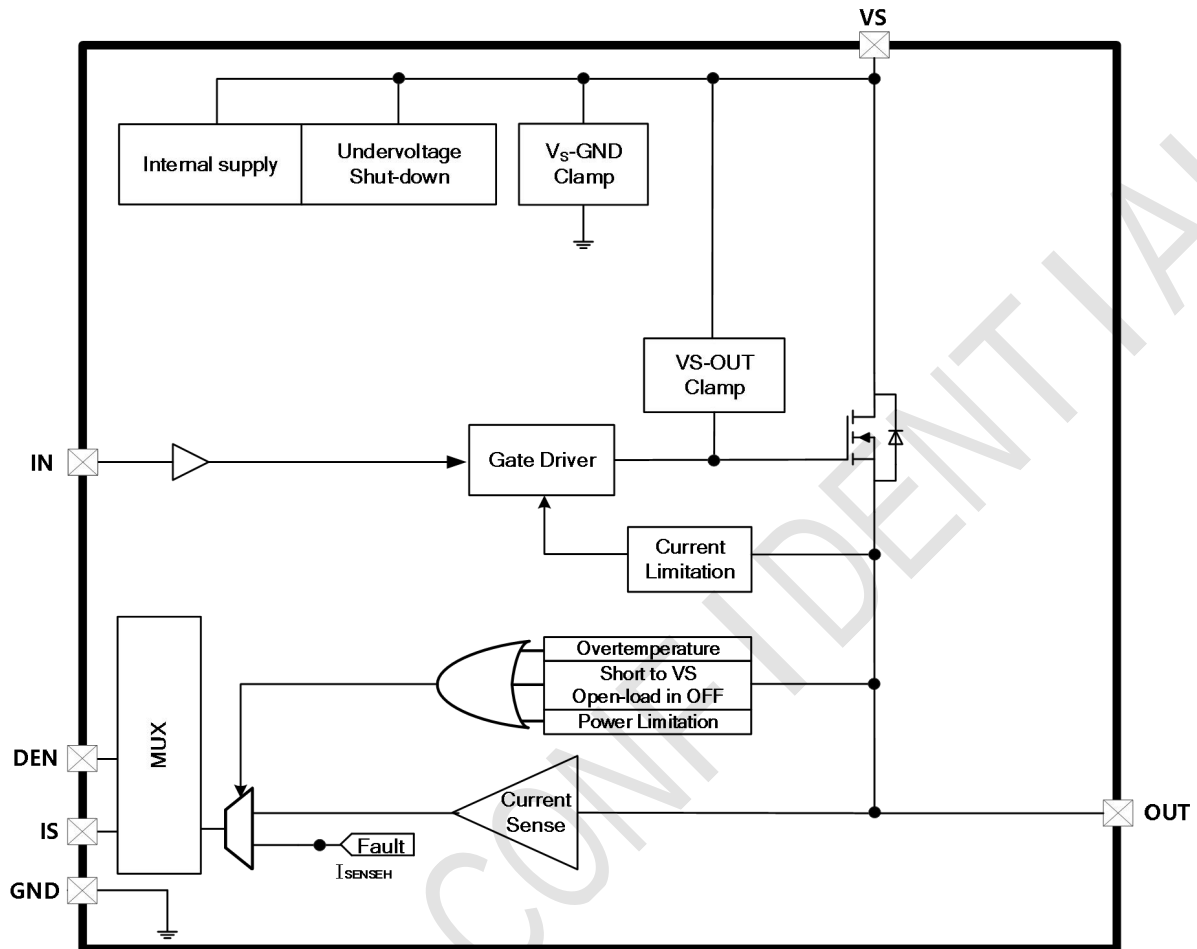
- 1) Not subject to production test - specified by design.
- 2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.
- 3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002.
- 4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011.

EAS Susceptibility (Note7)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse			300	mJ	$I_{OUT} = 12A$ $T_{J(0)} = 150\text{ }^{\circ}C$ $V_S = 28\text{ V}$

Note7: Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note8), $8V < V_S < 36V$; $-40^{\circ}C < T_J < 150^{\circ}C$, unless otherwise specified**Power section**

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		8	24	36	V
Extended operating voltage	V_{OP}		5		58	V
Under voltage shutdown	V_{USD}			3.5	5.0	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	$I_{OUT}=5A, T_J = 25^{\circ}C$		9		mΩ
		$I_{OUT}=5A, T_J = 150^{\circ}C$			18	
		$I_{OUT}=5A, V_S=5V, T_J = 25^{\circ}C$			14	
Nominal load current	$I_{L(NOM)}$	$T_A=25^{\circ}C$		13		A
Nominal load current at $T_A=85^{\circ}C$	$I_{L(NOM)_85}$	$T_A=85^{\circ}C, T_J < 150^{\circ}C$		10		A
Inverse Current Capability	$I_{L(INV)}$	$V_S < V_{OUT}, V_{IN}=5V, T_A=25^{\circ}C$		13		A
V_S clamp voltage	V_{CLAMP}	$I_S=20\text{ mA}$	60	64	71	V
Supply current in sleep	I_{SLEEP}	$V_S=36V, V_{IN}=V_{OUT}=V_{DEN}=0V, T_J=25^{\circ}C$		3.0	6.0	μA
		$V_S=36V, V_{IN}=V_{OUT}=V_{DEN}=0V, T_J=125^{\circ}C$			20	μA
Sleepy mode blanking time	t_{D_SLEEP}	$V_S=36V, V_{IN}=V_{OUT}=0V$ $V_{DEN}=5V$ to $0V$	150	400	800	us
Supply current in active	$I_{S(ACTIVE)}$	$V_S=36V, V_{DEN}=5V, V_{IN}=0V,$		1.2	2.5	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	$V_S=36V, V_{DEN}=5V, V_{IN}=5V$		5.0	10	mA
Off-state output current	$I_{L(off)}$	$V_{IN}=V_{OUT}=0V, V_S=36V, T_J=25^{\circ}C$		0.1	3	μA
		$V_{IN}=V_{OUT}=0V, V_S=36V, T_J=125^{\circ}C$			20	μA
OUT - V_S diode voltage	V_F	$I_{OUT}=-2A, T_J=150^{\circ}C$			0.9	V

Bypass mode

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Bypass mode load current	$I_{L(bypass)}$	$V_S=28V, V_{OUT}=V_S-2V$	140	200	260	mA
Operating current in bypass mode	$I_{GND(bypass)}$	$V_S=28V, V_{IN}=0V$		70	100	uA
Number of DEN pluses to bypass mode	n_{DEN_valid}	$V_S=28V$		8		cycles
High level enable detection pulse width of DEN	T_{ENH}	$V_S=28V$	1.3	1.5	1.7	ms
Low level enable detection pulse width of DEN	T_{ENL}	$V_S=28V$	100		400	us
Bypass mode writing time	T_{DEN_WRITE}	$V_S=28V$			20	ms
High level detection pulse width of IN	T_{INH}	$V_S=28V$	100			us
Bypass mode IN writing time	T_{IN_WRITE}	$V_S=28V$			1.2	ms
High level disable detection pulse width of DEN	T_{DISH}	$V_S=28V$	5			ms

Switching						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at $T_j = 25^\circ\text{C}$	$T_{d(on)}$	$V_S=28\text{V}, V_{DEN}=5\text{V}, R_L=6\Omega$		20	80	μs
Turn-off delay time at $T_j = 25^\circ\text{C}$	$T_{d(off)}$			35	100	μs
Turn-on voltage slope at $T_j = 25^\circ\text{C}$	$(dV_{OUT}/dt)_{on}$	$V_S=28\text{V}, V_{DEN}=5\text{V}, R_L=6\Omega$	0.2	0.5	1.0	V/ μs
Turn-off voltage slope at $T_j = 25^\circ\text{C}$	$(dV_{OUT}/dt)_{off}$		0.2	0.5	1.0	
Differential pulse skew($t_{PHL} - t_{PLH}$)	t_{SKEW}	$V_S=28\text{V}, V_{DEN}=5\text{V}, R_L=6\Omega$	-50		50	μs
Logic input (IN, DEN)						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	$V_{LOW}=0.9\text{V}$	2	11	35	μA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V
High level logic input current	I_{HIGH}	$V_{HIGH}=2.0\text{V}$	1	10	32	μA
Logic input hysteresis voltage	$V_{(hyst)}$			0.2		V
Protections						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	$5\text{V} < V_S < 36\text{V}, V_{DS}=6\text{V}$	52	75	88	A
		$V_{DS}=32\text{V}$		40		
Short circuit current during thermal cycling	I_{LIML}	$V_S=24\text{V}, V_{DEN}=5\text{V}, T_R < T_j < T_{TSD}$		20		
Maximum number of Short mode latch				5		cycles
Shutdown temperature	T_{TSD}		150	175	200	$^\circ\text{C}$
Thermal hysteresis	T_{HYST}			20		$^\circ\text{C}$
Current limit reset temperature	T_R			135		$^\circ\text{C}$
Dynamic temperature	ΔT_{J_SD}	$T_j = -40^\circ\text{C}$		60		$^\circ\text{C}$
Turn-off output voltage clamp	V_{DEMG}	$I_{OUT}=2\text{A}, V_{DEN}=5\text{V}, L=6\text{mH},$ $T_j = -40^\circ\text{C} \text{ to } 150^\circ\text{C}$	V_S-60	V_S-64	V_S-71	V
Current sense characteristics						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
I_{OUT}/I_{IS}	K_0	$I_{OUT}=50\text{mA}, V_{DEN}=5\text{V}$	-15%	1960	+15%	
I_{OUT}/I_{IS}	K_1	$I_{OUT}=0.5\text{A}, V_{DEN}=5\text{V}$	-5%	4610	+5%	
I_{OUT}/I_{IS}	K_2	$I_{OUT}=2\text{A}, V_{DEN}=5\text{V}$	-3%	5250	+3%	
I_{OUT}/I_{IS}	K_3	$I_{OUT}=4\text{A}, V_{DEN}=5\text{V}$	-3%	5250	+3%	
I_{OUT}/I_{IS}	K_4	$I_{OUT}=10\text{A}, V_{DEN}=5\text{V}$	-3%	5250	+3%	
K derating with temperature	ΔK		-2%	0	+2%	
Current sense leakage current	I_{ISO}	IS disabled: $V_{DEN}=0\text{V}$	0		1	μA
		IS enabled: $V_{DEN}=5\text{V}, \text{channel ON}, I_{OUT}=0\text{A}$		15		

Output voltage for IS shutdown	V_{OUT_MSD}	$V_{DEN}=5V$, $R_{SENSE}=3.9K$, $V_{IN}=5V$; $I_{OUT}=6A$		5		V
Max analog sense output voltage	V_{IS}	$V_S=28V$, $V_{IS}=5V$	4.5			V
Current sense output current in fault condition	I_{ISH}	$V_S=28V$, $V_{IS}=5V$	10	20	30	mA
Current sense output voltage in fault condition	V_{ISH}	$V_S=28V$, $V_{IS}=5V$	5.4	6	6.6	V

OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold	V_{OL}	$V_{DEN}=5V$, $V_{IN}=0V$	2	3.5	5	V
OFF-state output sink current	$I_{L(off2)}$	$V_S=28V$, $V_{IN}=0V$, $V_{OUT}=V_{OL}$, $T_j = -40^{\circ}C$ to $150^{\circ}C$		-50		μA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	$V_{DEN}=5V$, $V_{OUT}=5V$, $V_{IN}=5V$ to $0V$	150	400	800	μs
Settling time for valid OFF-state open load diagnostic indication from rising edge of DEN	$t_{D_OL_V}$	$V_{IN}=0V$, $V_{OUT}=5V$, $V_{DEN}=0V$ to $5V$			150	μs
OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	$V_{DEN}=5V$, $V_{IN}=0V$, $V_{OUT}=0V$ to $5V$		5	30	μs

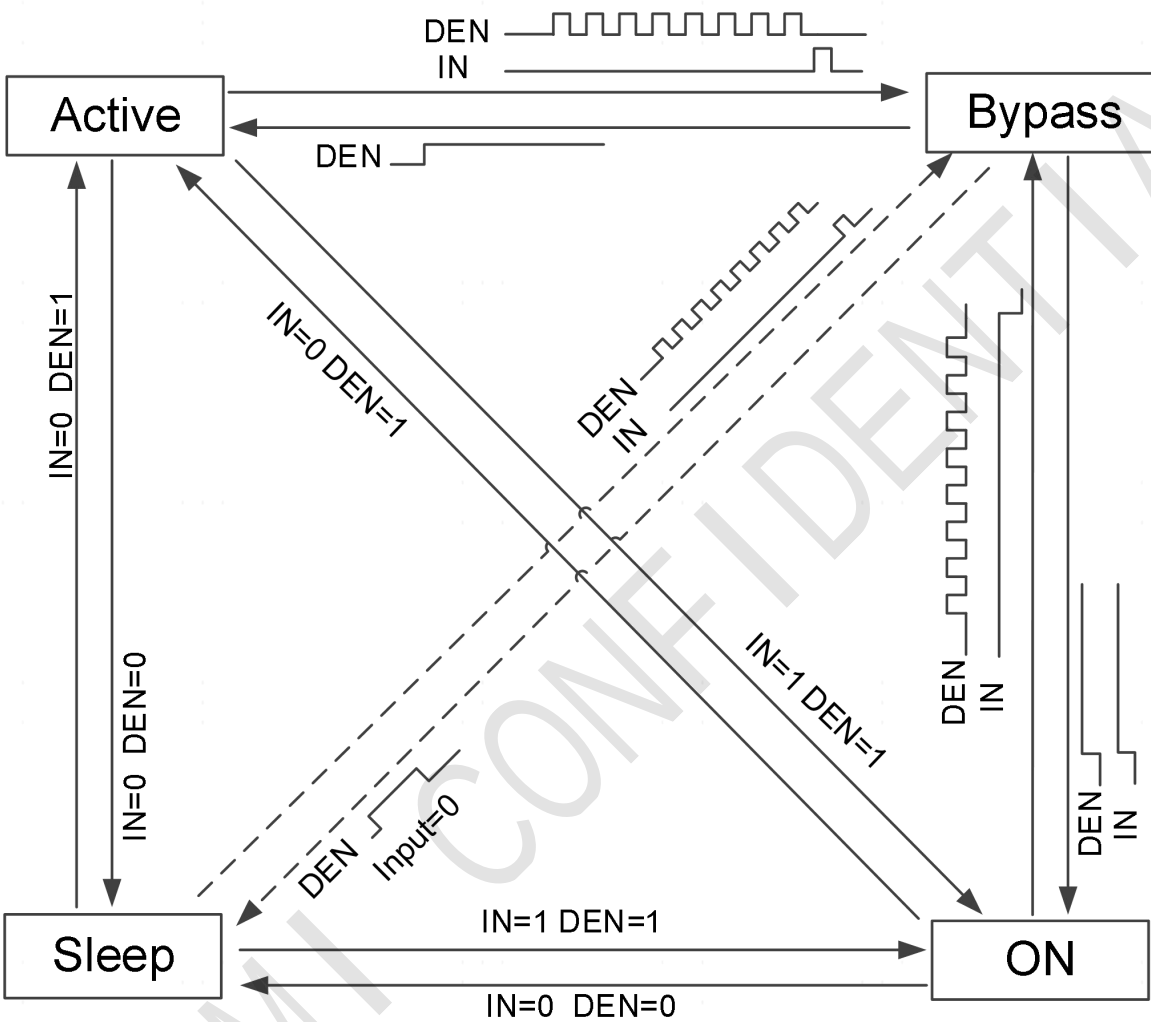
Current sense timings

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense settling time from rising edge of DEN	$t_{DSSENSE1H}$	$V_{IN}=5V$, $V_{DEN}=0V$ to $5V$, $R_{SENSE}=1K$, $R_L=6\Omega$			100	μs
Current sense disable delay time from falling edge of DEN	$t_{DSSENSE1L}$	$V_{IN}=5V$, $V_{DEN}=5V$ to $0V$, $R_{SENSE}=1K$, $R_L=6\Omega$		5	20	μs
Current sense settling time from rising edge of IN	$t_{DSSENSE2H}$	$V_{IN}=0V$ to $5V$, $V_{DEN}=5V$, $R_{SENSE}=1K$, $R_L=6\Omega$		80	250	μs
Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$\Delta t_{DSSENSE2H}$	$V_{IN}=5V$, $V_{DEN}=5V$, $R_{SENSE}=1K$, $I_{IS}=90\%$ of I_{IS_MAX} , $I_{OUT}=90\%$ of I_{OUTMAX} , $R_L=6\Omega$			150	μs
Current sense turn-off delay time from falling edge of IN	$t_{DSSENSE2L}$	$V_{IN}=5V$ to $0V$, $V_{DEN}=5V$, $R_{SENSE}=1K$, $R_L=6\Omega$		80	250	μs

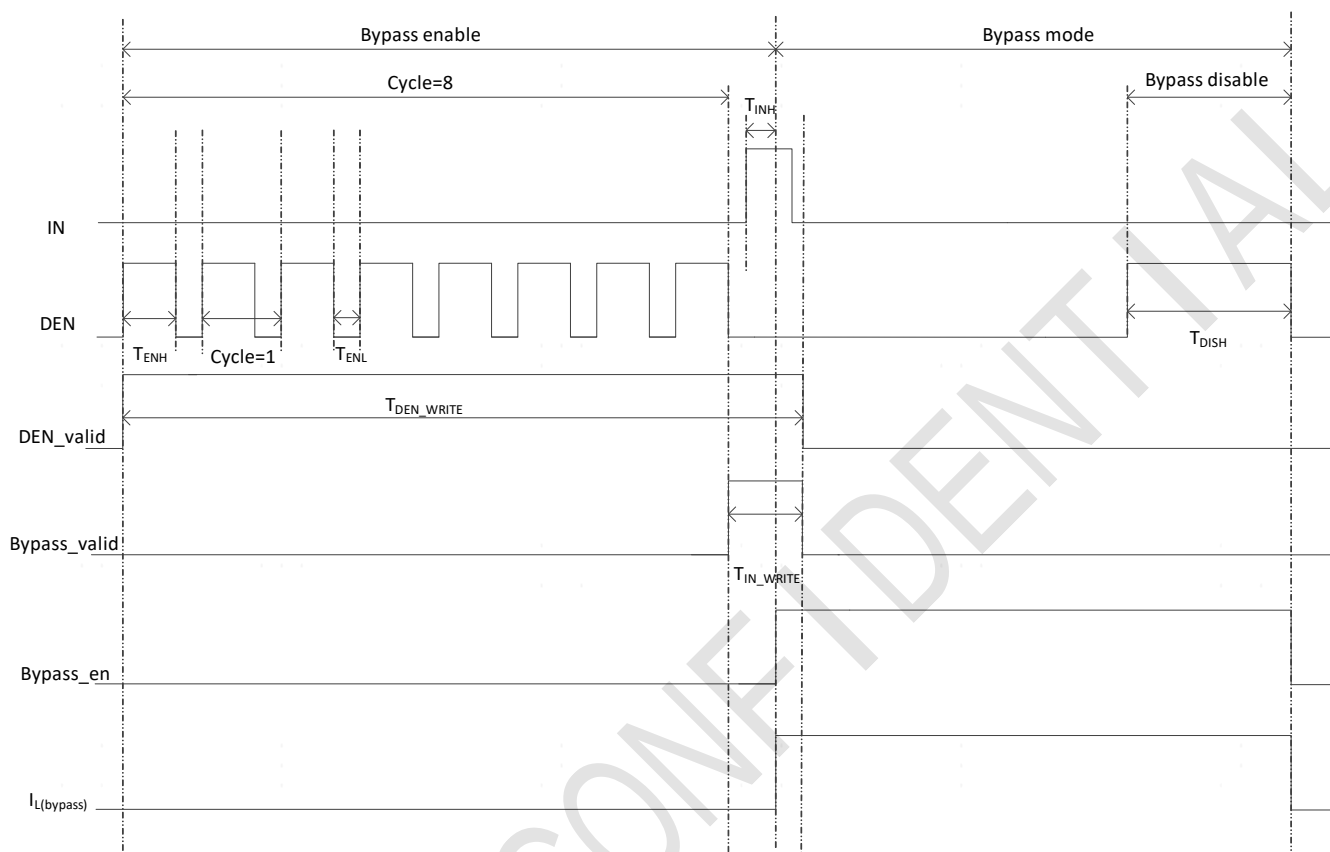
Note8: Except for the special test instructions, all electrical parameters are tested under $T_A = +25^{\circ}C$. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis

Operation modes

State machine



Bypass mode



Bypass mode enable:

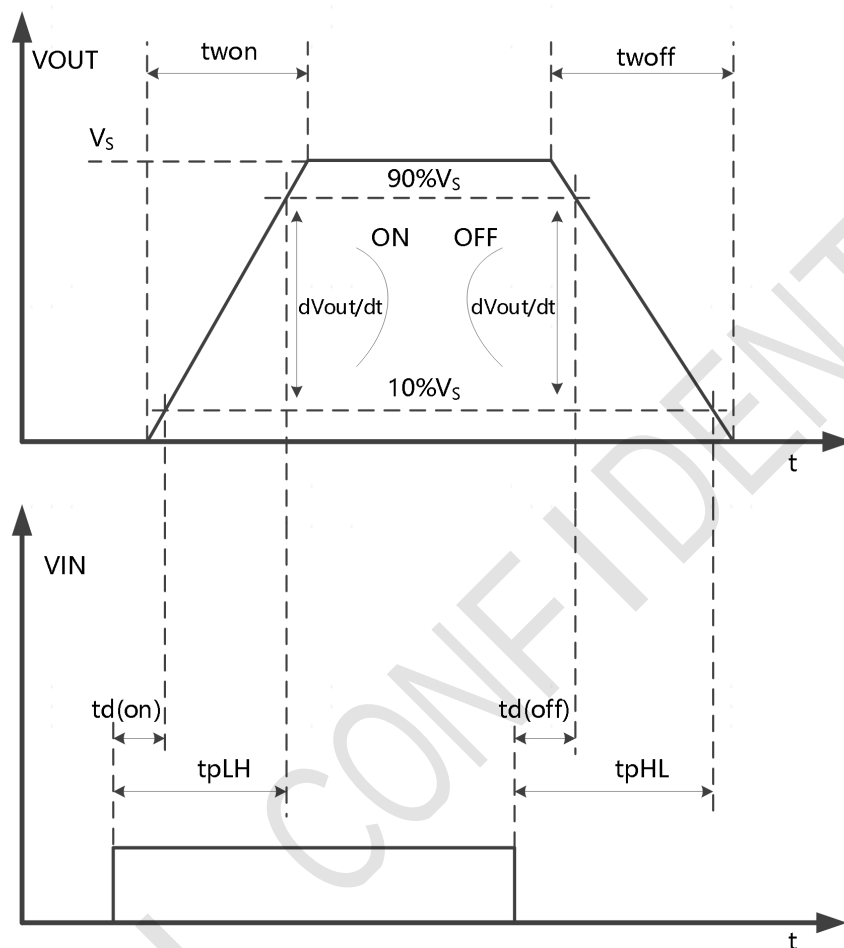
The valid input signal of DEN ($T_{ENH}=1.5\text{ms}$ & $T_{ENL}=100\mu\text{s}$), with 8 consecutive cycles input from the first rising edge within 20ms (T_{DEN_WRITE}), and a valid pulse of IN ($T_{INH}>100\mu\text{s}$) inputs from the falling edge of the 8th cycle within 1.2ms (T_{IN_WRITE}), enables the bypass mode (Bypass_en=H), which can offer 200mA load current of Maximum. Otherwise, it is not possible to enable bypass mode.

Bypass mode disable:

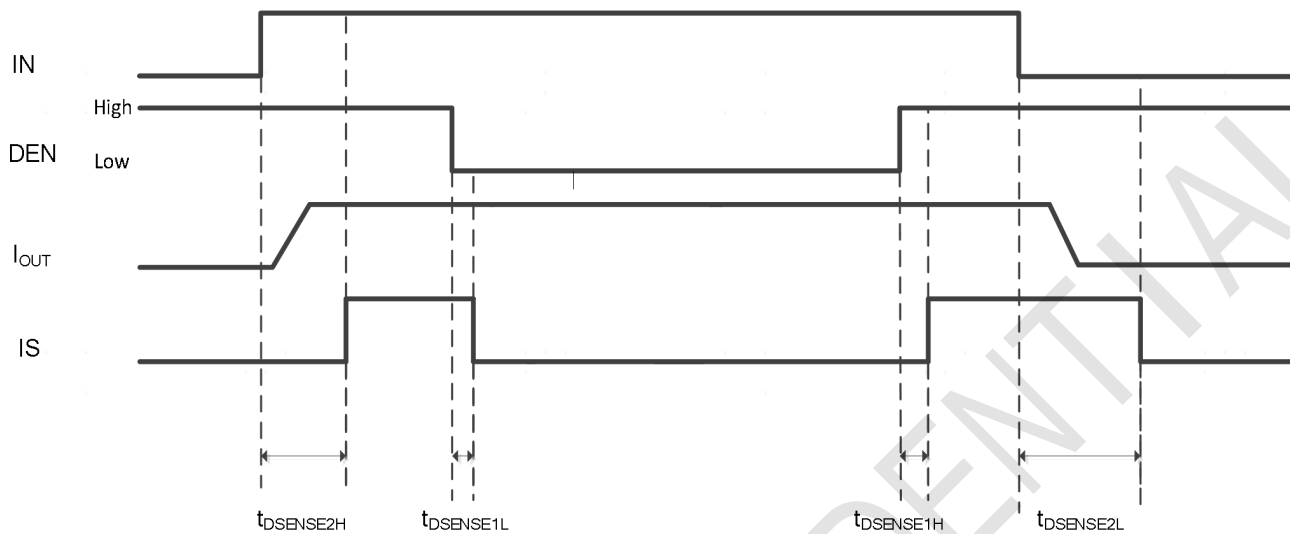
After enabling bypass mode, it can be disabled by a valid high level signal of DEN ($T_{DISH}>5\text{ms}$).

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

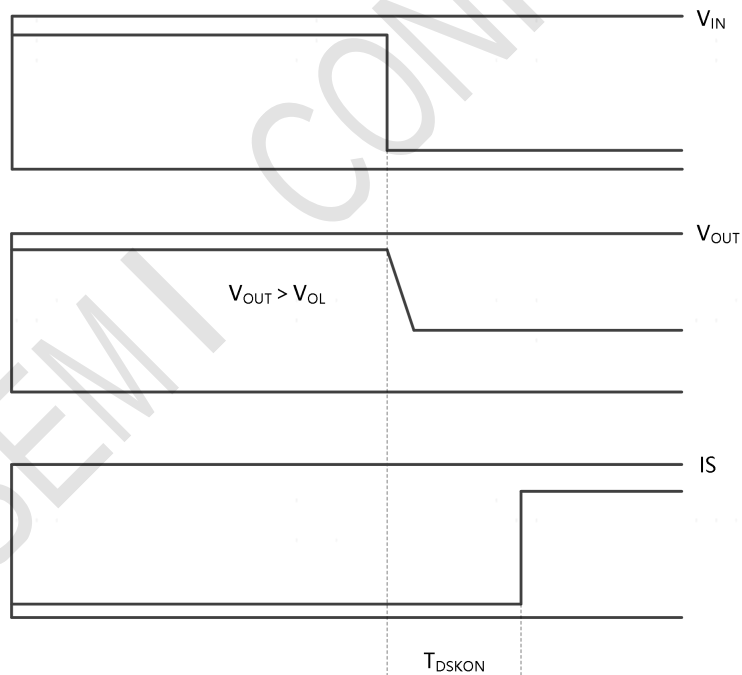


Table 2. Truth table

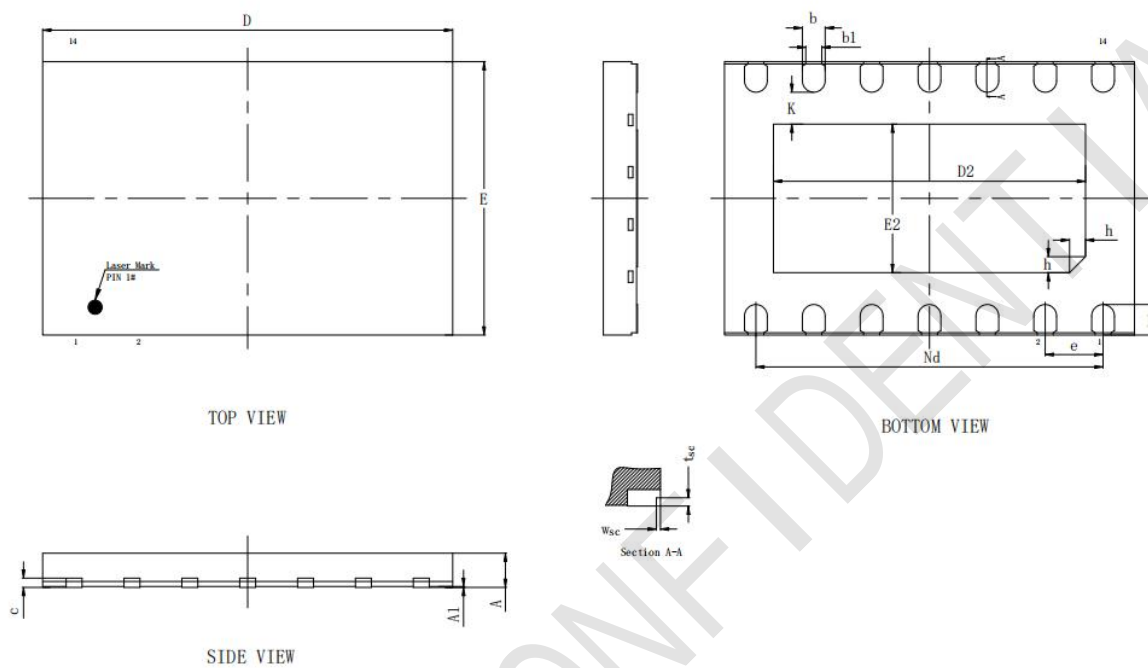
Conditions	IN	DEN	OUT	IS
Standby	L	L	L	0
Normal	L	H	L	0
	H	H	H	$I_{IS} = I_{OUT}/K$
Overload	H	H	H	I_{ISH}
OverTemperature	L	H	L	0
	H	H	Latched	I_{ISH}
Undervoltage	X	X	L	0
Short to V_S	L	H	H	I_{ISH}
	H	H	H	<Normal
Open-Load	L	H	H	I_{ISH}
Short circuit to GND	H	H	L	I_{ISH}

Table 3. Current sense output

DEN	MUX Channel	Current sense output			
		Normal	Overload	OFF-state	Negative output
L		Hi-Z			
H	Channel diagnostic	$I_{IS} = I_{OUT}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z

Package Outline

DFN9×6-14L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.45	0.50	0.55
b1	0.35REF		
c	0.203REF		
D	8.90	9.00	9.10
D2	6.75	6.85	6.95
e	1.27BSC		
Nd	7.62BSC		
E	5.90	6.00	6.10
E2	3.16	3.26	3.36
L	0.62	0.67	0.72
h	0.30	0.35	0.40
K	0.70REF		
W _{sc}	0.01	-	0.09
t _{sc}	0.08	-	0.18

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